NEC

User's Manual
16M-Bit Synchronous DRAM
μPD4516421, 4516821, 4516161

June 1995

Document No. M10187EU1V0UM00

NEC

16M-Bit Synchronous DRAM User's Manual

Document Number M10187EU1V0UM00

First Printing: June 1995

NEC

Contents

Figure **Page**

Figure **Page**

NEC

Introduction 1

1.1 Speed Revolution

In the past two decades, dynamic RAM densities have increased from 1 Kbit per chip to more than 256 Mbits per chip, a factor of over 256,000. DRAM performance has not kept the same pace as these density changes; access times have only improved by a factor of 10. The market demand to lower the price per bit far exceeded the demand for improved access times as designers utilized primary and secondary cache memory structures to circumvent the long DRAM access latencies.

During this same 20-year period, microprocessor performance improved by two orders of magnitude. The new reduced instruction set computers (RISC) with their attendant superscalar architecture require at least twice the bus bandwidth as the older complex instruction set computers (CISC) due to the spawning of multiple instructions per clock tick.

Multiprocessor-based RISC systems have only added additional bandwidth requirements. It became evident at the beginning of this decade that main memory required at least an order of magnitude improvement in bandwidth or that much larger high-performance cache memories be applied if the performance gains of the emerging CPU architectures were to be maintained. (Figure 1-1). This, in essence, was the driving force behind the development of the synchronous DRAM.

The reasons for the main memory performance bottleneck are related to device geometry, switching at the interfaces, and transmission line reflections. The performance of modern CPUs mainly depends on the ever-decreasing geometries of the CMOS-based DRAM. Historically, the smallest geometries have been delivered first in the form of DRAMs. Horizontal and vertical scaling of these devices has enabled lower voltage supplies and higher operating frequencies.

Simultaneous switching of push-pull transistors at the external interface causes high instantaneous power excursions. The slew rate control to limit this excursion and the electrostatic discharge protection circuitry both delay the switching characteristics of the input/output structures

Transmission line reflections from the less-than-ideal external multiple-stub environment is a particular concern of the systems designer.

1.2 Advantages of Synchronous DRAMs

The synchronous DRAM (SDRAM) derives its name from the fact that all of the input signals, called commands, are accepted by the device on the rising edge of the clock signal (“synchronized” with the clock). The clock allows data pipelining within the device and data output in a continuous stream.

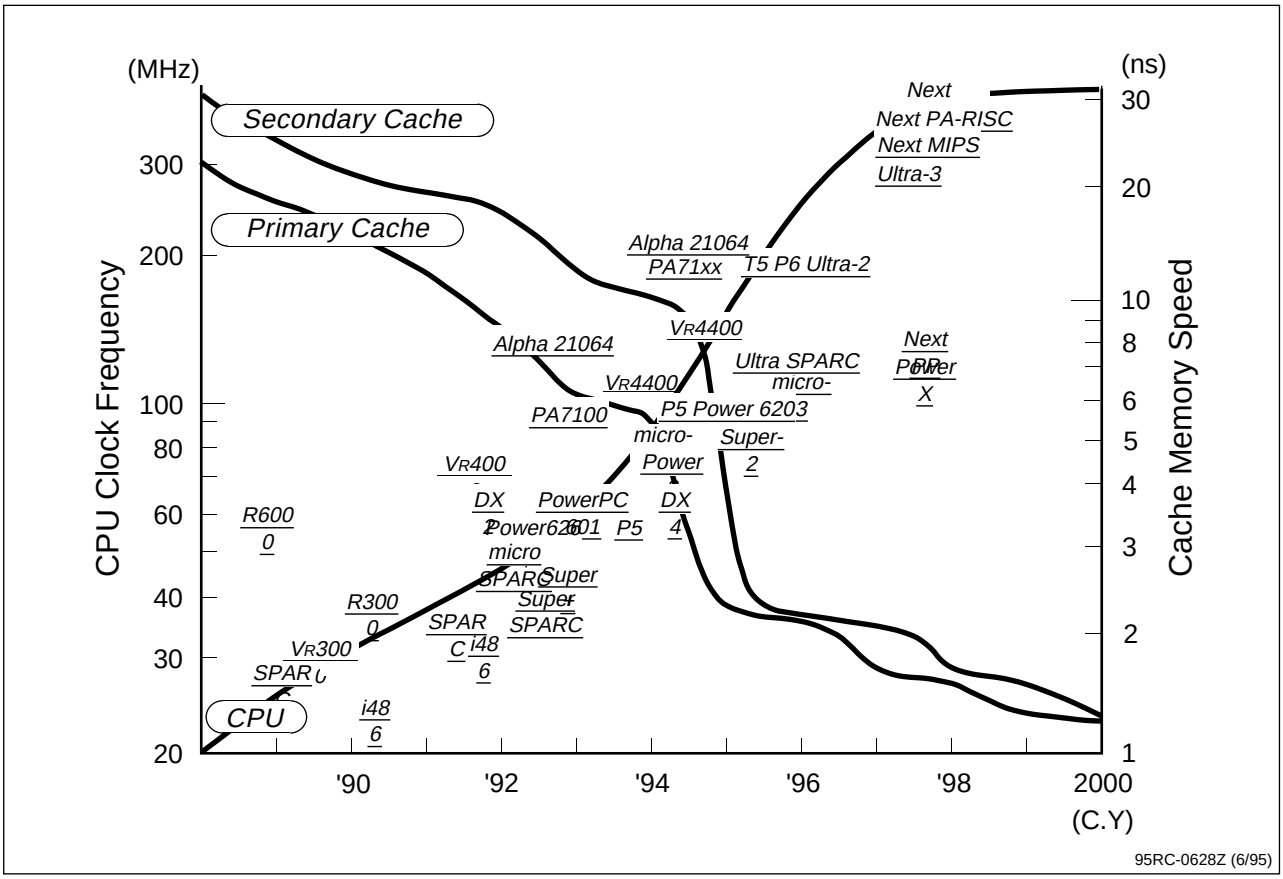
Advantages of synchronous DRAMs over fast-page mode DRAMs stem from three major advances in memory and semiconductor technology. The first is the use of a double-metal process developed by NEC for 16-Mb DRAMs. Here, interconnects over the memory cell array allow the highly-parallel sense amplifiers to be used as a high-speed cache. Random data access on an active row occurs on each clock edge, yielding a cycle time of 10 nanoseconds.

The second innovation is the application of a directly connected system clock with an internal state machine to control the fully pipelined operation of the memory. This eliminates internal “self-timed” circuitry, enabling higher throughput, improved testability, and better yields in a high-volume production environment.

The third innovation involves the physical interface levels and power supply voltages. The NEC synchronous DRAM is designed to use the JEDEC standard 3.3-volt Vdd supply with the data I/O designed to the standard low voltage TTL interface (LVTTL), internally regulated to 2.5 volts for the internal DRAM array. Both contribute to lowering the individual device power budget over the older 5-volt power supply for TTL standard devices.

The NEC synchronous DRAM is available in the thin, small-outline package, type II (TSOP2), JEDEC standard.

Figure 1-1. CPU Clock Frequency vs Cache Memory Speed



NEC

Basic Functions 2

2.1 Features

2.1.1 Synchronization

Synchronizing the memory device with the clock has the advantage that all signals going to the memory device meet the same requirements with respect to the clock as most other components in the system. With the SDRAM, most control logic in the memory system that was used to synchronize data from the memory with the system clock may now be eliminated.

2.1.2 Two-Bank Structure

Having two banks allows two operations to be in progress simultaneously; for example, outputting data from one bank while the other bank is being precharged. This significantly reduces system latency.

Also, many systems are designed with multiple memory banks. Having the interleaving logic on the memory devices reduces the complexity of the system because it is no longer required externally.

2.1.3 Burst Transfers

The SDRAM has the ability to output a fixed number of memory locations on successive clocks. This makes it very easy to fill a cache with a fixed cache line length. Since commands to the memory device are not required for each transfer in the burst, system complexity is reduced.

2.2 Comparison With Conventional DRAM

Figure 2-1 shows the basic actions by the SDRAM in comparison with a conventional DRAM, which has $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, and $\overline{\text{OE}}$ input pins. Signal levels and timing control the actions at these pins.

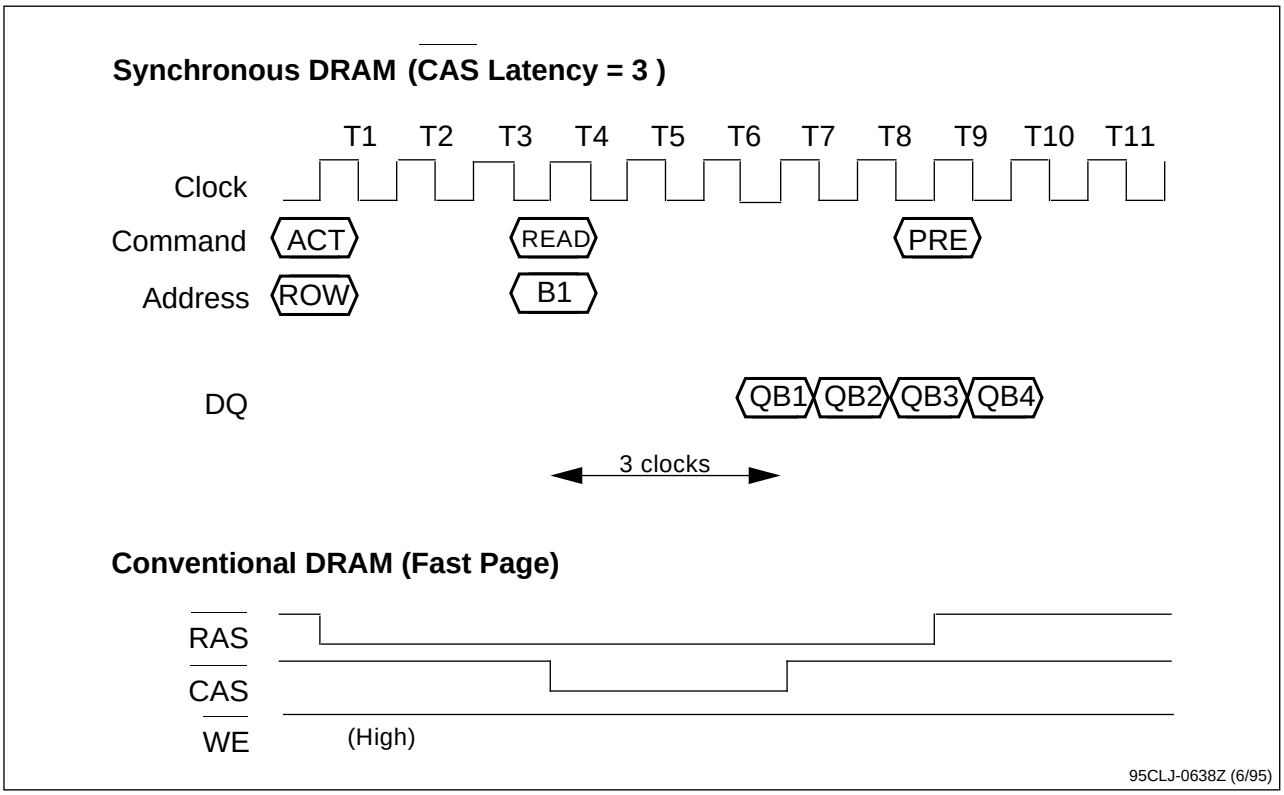
In the SDRAM, external signals are latched with the positive edge of the clock pulses, and particular high and low combinations are recognized as commands.

(10) The activate command (ACT) corresponds to $\overline{RAS}$ falling of the data with a sense amplifier.

(11) The read command (READ) corresponds to $\overline{CAS}$ falling and serves to read out the column address (B1) data.

(12) The precharge command (PRE) corresponds to $\overline{RAS}$ rising and starts the precharging.

Figure 2-1. Synchronous DRAM Comparison With Conventional DRAM



2.3 State Diagram Definitions

Figure 2-2 is a simplified state diagram of the SDRAM. Each circle represents a state of the SDRAM, and commands or conditions on the lines represent an external input.

Idle. All actions start from the idle state. This state is the same as the precharged standby state. If the precharge command (PRE) is asserted, the SDRAM automatically goes to this state after tRP.

Row Active. The row active state is when a row address has been selected but no action (such as a read or write command) has been requested. To transition from the idle state to this state, the activate command (ACT) with the row address must be asserted.

Read, Write. The SDRAM will be in a read or write state when the device is performing a read or write operation. Once the read or write is completed, the device will automatically return to the row active state unless auto precharge was also active, in which case it will return to the idle state.

Read Suspend, Write Suspend, ReadA Suspend, WriteA Suspend. During a read or write, if the clock enable pin (CKE) goes low, the SDRAM suspends the operation.

ReadA, WriteA. If a read with auto or write precharge command is asserted, the SDRAM automatically goes to the precharge state and then goes to the idle state after the read or write actions.

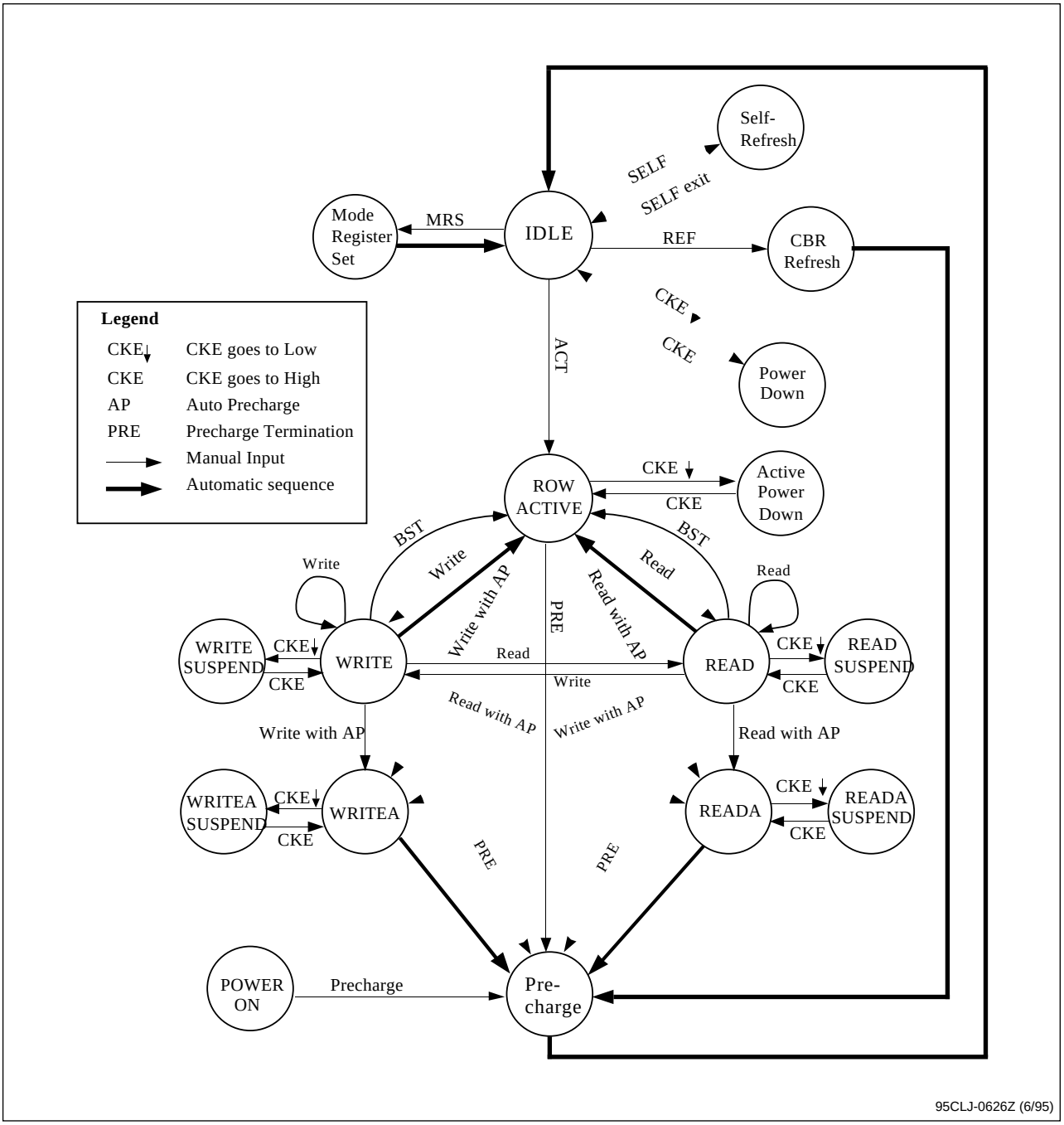
Mode Register Set. The mode register may be written when in the idle state. Two clocks after completion of the write, the SDRAM will return to the idle state.

CBR Refresh. During CBR refresh, the SDRAM will refresh two rows, one in each bank. Before executing the CBR command, both banks must be in the idle state. After completion of the refresh, a precharge will be executed and the SDRAM will return to the idle state.

Self-Refresh. The SDRAM has a low-power standby state called self-refresh. This state is entered when the CBR refresh is executed and CKE is low. While the SDRAM is in self-refresh, the device will automatically refresh itself. No user-executed refresh cycles are needed during this time. To exit self-refresh, the CKE line is brought high and the SDRAM returns to the idle state.

Power-Down, Active-Power-Down. Both power-down and active-power-down modes are entered by bringing CKE low when either in the idle state or the row-active state, respectively. While in this mode, all input buffers except CKE are turned off. This reduces the amount of power required by the SDRAM. When CKE is brought high, the device will return to its previous state, either the idle or row-active state.

Figure 2-2. Simplified State Diagram



2.4 Pipeline Implementation

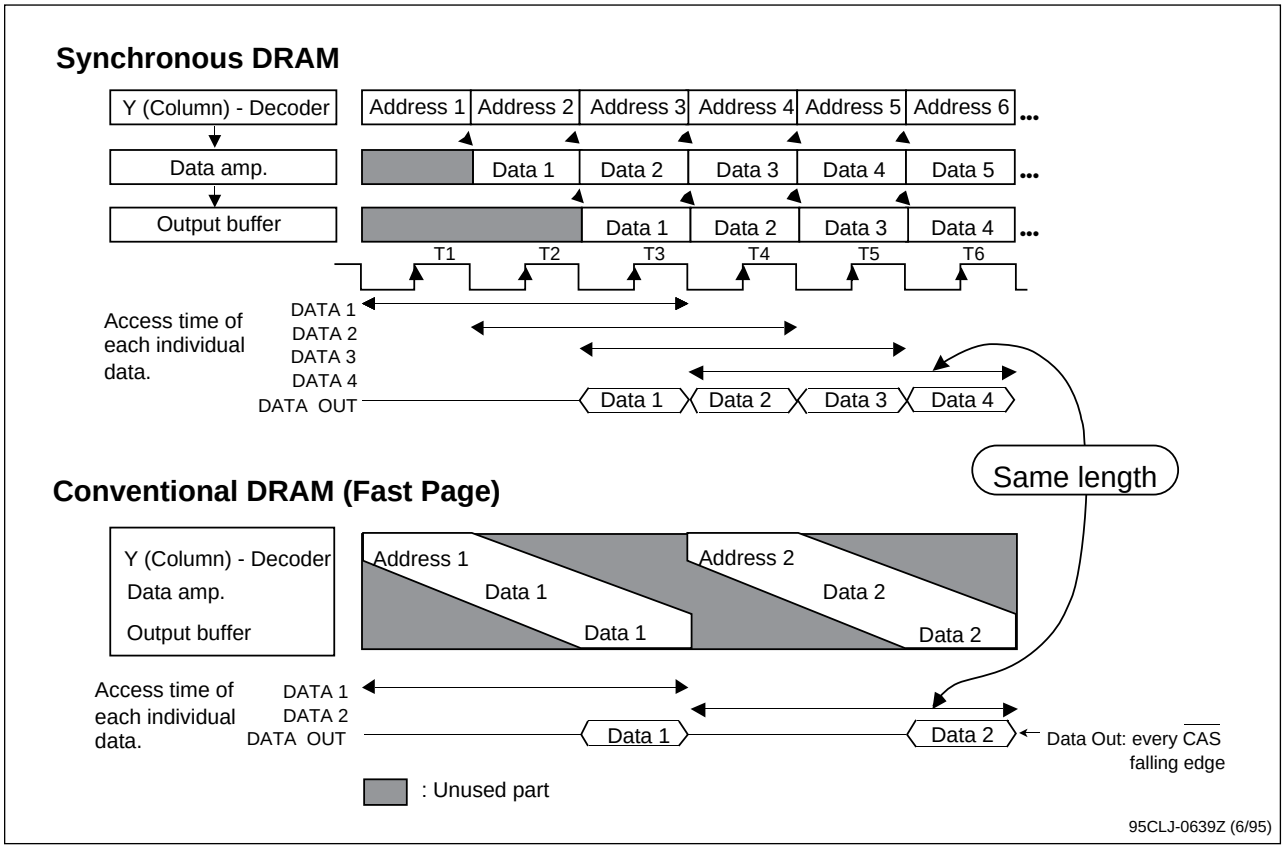
2.4.1 Concept of the Pipeline

The pipeline circuit technology was introduced to increase the data transfer speed by dividing the series of column side actions and parallel actions of each divided block.

In the NEC 16-Mb SDRAM, the column side actions are divided into three steps by the clock.

Figure 2-3 shows the concept of the three-stage pipeline architecture in comparison with conventional DRAMs. In the conventional DRAM, the column side actions from a column address input to the corresponding data output are series actions. Whereas in the SDRAM, the column side actions are divided into three blocks that act in parallel.

Figure 2-3. Pipeline Concept



2.4.2 Three-Stage Pipeline Circuit

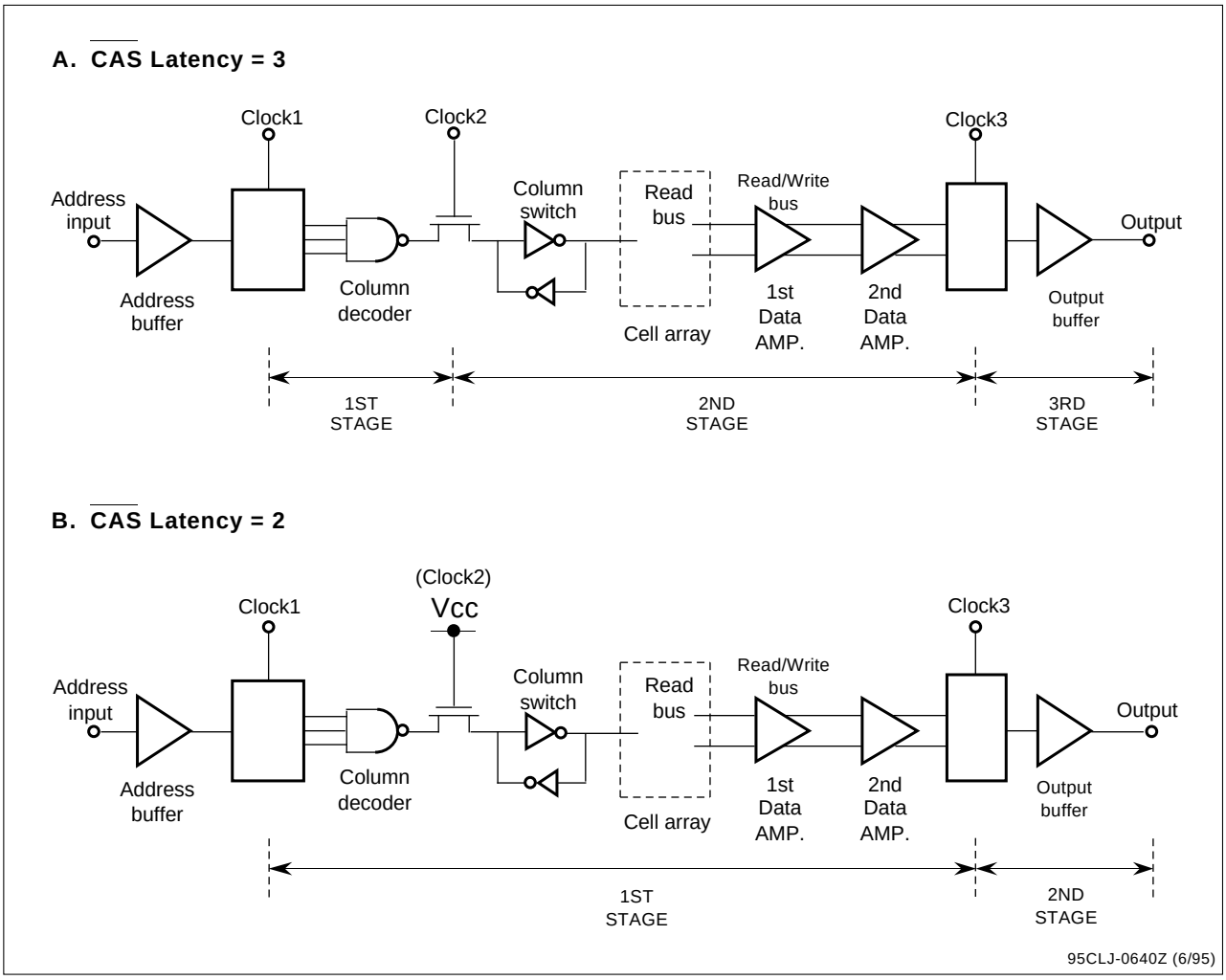
Figure 2-4 is a three-stage pipeline circuit for $\overline{CAS}$ latencies of 3 and 2. The column side actions are divided into three stages: the first is from external address latching to column switch selection; the second is from column switch selection to data output buffer latching; and the third is from output buffer activation to the DQ pin output completion. The three stages are divided by input clock pulses, and the internal actions are multiplexed.

As a result, although the time required for each data is the same as the first access time, the total data transfer rate for plural words is greatly reduced by the multiplex operation.

For the $\overline{CAS}$ latency of 2, the transmission gate is continuously turned on. On the first clock, the column address is latched, ripples through the column decoder, and selects the appropriate column switch. The corresponding data is fed to the amplifiers and waits at the output buffer for the second clock. When the second clock comes, the data is strobed into the output buffer and onto the data bus.

For the $\overline{CAS}$ latency of 1, the transmission gate is again continuously turned on. In addition, the output buffer becomes a transparent latch. It is almost the same as the access path of the conventional DRAM.

Figure 2-4. Address Access Pass

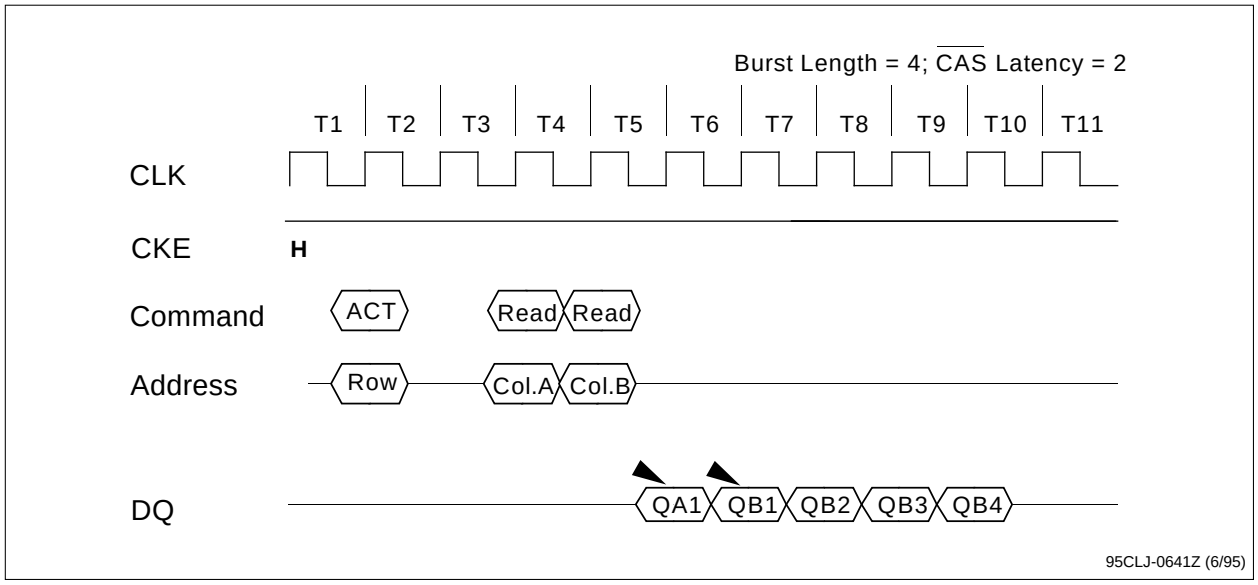


2.4.3 Advantages of Pipeline

The pipeline circuit architecture has several advantages over other methods for high-speed data transfer. One of the most significant advantages is that the preceding burst transfer can be terminated by re-inputting a read/write command at the timing of any cycle during the burst mode.

In the case of a read cycle with a burst length of 4 and $\overline{\text{CAS}}$ latency of 3 (Figure 2-5), the burst action by the first read command (A address) will be terminated at T6 when a new read command (B address) is asserted at T5. The new burst action by the B address will begin at T7. The key point is that there is no restriction on changing a column address.

Figure 2-5. Pipeline Advantage



2.5 Package Pin Functions

Table 2-1. Package Pin Functions

Symbol	Input/Output	Function
A0 - A10	Input	A0 - A10 is the row address for all organizations of the SDRAM during a cycle. During a command, these bits are the column address as shown below: A0 - A9 for x4 organization A0 - A8 for x8 organization A0 - A7 for x16 organization A10 defines the precharge mode. When A10 is high in the precharge command cycle, both banks are precharged; when A10 is low, only the bank selected by A11 is precharged. During a read or write command cycle, A10 controls auto-precharge. If A10 is high, then a precharge will automatically start after the burst access has completed.
A11	Input	A11 is the bank select signal (BS). During a command cycle, A11 low selects bank A and A11 high selects bank B.
CKE	Input	CKE controls both the internal clock and power-down mode. During a burst read or write, if CKE is high, an internal clock will be generated. If CKE is low, then the next clock will be skipped and the device will be suspended until one clock after CKE goes high again. If CKE is low during the rising edge of the clock and the device is in the idle state, then power-down mode will be entered. When CKE returns high, the device will exit power-down mode.
CLK	Input	CLK is the master clock input. All signals are referenced to the rising edge of CLK.
CS	Input	$\overline{CS}$ (Command Select) low starts the command input cycle. When $\overline{CS}$ is high, commands are ignored, but previously initiated commands will continue.
DQM, DQMU, DQML	Input	DQM controls the I/O buffers. In x16 products, DQMU and DQML control upper and lower bytes, respectively. During a read burst, DQM controls whether the output buffers are driving the bus or are in a high-impedance state. This is similar to the $\overline{OE}$ pin on a standard DRAM. The DQM latency for the read is 2 clocks. During a write burst, DQM controls the word mask. Input data is written to the memory cells if DQM is low but not if DQM is high. The DQM latency is zero for a write and 2 clocks for a read.
I/O0 - I/O15	I/O	During read bursts, output data appears on pins I/O0 - I/O15. During write bursts, the device accepts input data from I/O0 - I/O15. The function of these pins is the same as on a conventional DRAM.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	$\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ individually have functions similar to a conventional DRAM. However, when a combination of these signals is used, there are some differences. Please refer to the command table
Vdd, Vddq, Vss, Vssq		Vdd, Vss are power supply pins for internal circuits. Vddq and Vssq are power supply pins for the output buffers.

NEC

Command Structure 3

3.1 Command Table

The SDRAM is the first DRAM device whose operation is defined by a state diagram. The state diagram was not included in the JEDEC SDRAM standard because some vendors did not allow for fully pipelined operations in their designs. The truth table, in combination with the state diagram, determines the action taken by any particular command (truth table) and the next legal operation (state diagram). The truth table includes all possible command binary combinations for completeness.

The truth table for the SDRAM defines the standard interface states required to execute the standard operational functions (see Tables 3-1 through 3-6). Together, these tables can also be considered the SDRAM standard "Command" table in which the Current State column indicates the command function. The signals $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and an address define the input commands, which become active on the positive transition of the CKE input.

In the tables, H, L, and X mean high, low, and "don't care" levels; V means valid data input. In the CKE column, previous clock and current clock are "n–1" and "n," respectively.

Table 3-1. Command Truth Table

		CKE								
Function	**Symbol**	**n–1**	**n**	**$\overline{CS}$**	**$\overline{RAS}$**	**$\overline{CAS}$**	**$\overline{WE}$**	**A11**	**A10**	**A9-A0**
Device deselect	DESL	H	X	H	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X
Burst stop	BST	H	X	L	H	H	L	X	X	X
Read	READ	H	X	L	H	L	H	V	L	V
Read with auto precharge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with auto precharge	WRITA	H	X	L	H	L	L	V	H	V
Bank activate	ACT	H	X	L	L	H	H	V	V	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Mode register set	MRS	H	X	L	L	L	L	L	L	V

Table 3-2. DQM Truth Table

Function	Symbol	CKE n–1	CKE n	DQM U	DQM L
Data write/Output enable	ENB	H	X	L	
Data mask/Output disable	MASK	H	X	H	
Upper byte write enable/Output enable	ENBU	H	X	L	X
Lower byte write enable/Output enable	ENBL	H	X	X	L
Upper byte write inhibit/Output disable	MASKU	H	X	H	X
Lower byte write inhibit/Output disable	MASKL	H	X	X	H

Table 3-3. CKE Truth Table

Current State	Function	Symbol	CKE n–1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add
Activating	Clock suspend mode entry		H	L	X	X	X	X	X
Any	Clock suspend		L	L	X	X	X	X	X
Clock suspend	Clock suspend mode exit		L	H	X	X	X	X	X
Idle	CBR refresh command	REF	H	H	L	L	L	H	X
Idle	Self-refresh entry	SELF	H	L	L	L	L	H	X
Self-refresh	Self-refresh exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Idle	Power down entry		H	L	X	X	X	X	X
Power down	Power down exit		L	H	X	X	X	X	X

Table 3-4. Operative Commands

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Command	Action	Note
Idle	L	H	H	X	X	NOP or BST	Nop or power down	5
	H	X	X	X	X	DESL	Nop or power down	5
	L	H	L	H	BA,CA,A10	READ/ READA	ILLEGAL	3
	L	H	L	L	BA,CA,A10	WRIT/ WRITA	ILLEGAL	3
	L	L	H	H	BA,RA	ACT	Row active	
	L	L	H	L	BA,A10	PRE/PALL	Nop	
	L	L	L	H	X	REF/SELF	Refresh or self-refresh	6
	L	L	L	L	Op-Code	MRS	Mode register access	

Table 3-4. Operative Commands (cont)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Command	Action	Note
Row Active	H	X	X	X	X	DESL	Nop	
	L	H	H	X	X	NOP or BST	Nop	
	L	H	L	H	BA,CA,A10	READ/ READA	Begin read: determine AP	11
	L	H	L	L	BA,CA,A10	WRIT/ WRITA	Begin write: determine AP	11
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	Precharge	8
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Read	H	X	X	X	X	DESL	Continue burst to end → Row active	
	L	H	H	H	X	NOP	Continue burst to end → Row active	
	L	H	H	L	X	BST	Burst stop → Row active	
	L	H	L	H	BA,CA,A10	READ/ READA	Term burst, new read; determine AP	9
	L	H	L	L	BA,CA,A10	WRIT/ WRITA	Term burst, new read; determine AP	4, 9
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	Term burst, prechargeing	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write	H	X	X	X	X	DESL	Continue burst to end → Write recovery	
	L	H	H	H	X	NOP	Continue burst to end → Write recovering	
	L	H	H	L	X	BST	Burst stop → Row active	
	L	H	L	H	BA,CA,A10	READ/ READA	Term burst, start read; determine AP	4, 9
	L	H	L	L	BA,CA,A10	WRIT/ WRITA	Term burst, start read; determine AP	9
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	Term burst, prechargeing	10
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

Table 3-4. Operative Commands (cont)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Command	Action	Note
Read With Auto Precharge	H	X	X	X	X	DESL	Continue burst to end → Pre-charging	
	L	H	H	H	X	NOP	Continue burst to end → Pre-charging	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA,CA,A10	READ/ READA	ILLEGAL	
	L	H	L	L	BA,CA,A10	WRIT/ WRITA	ILLEGAL	
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write With Auto Precharge	H	X	X	X	X	DESL	Continue burst to end → Write recovering with auto pre-charge	
	L	H	H	H	X	NOP	Continue burst to end → Write recovering with auto pre-charge	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA,CA,A10	READ/ READA	ILLEGAL	
	L	H	L	L	BA,CA,A10	WRIT/ WRITA	ILLEGAL	
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Precharg-ing	H	X	X	X	X	DESL	Nop → Enter idle after tRP	
	L	H	H	H	X	NOP	Nop → Enter idle after tRP	
	L	H	H	L	X	BST	Nop → Enter idle after tRP	
	L	H	L	H	BA,CA,A10	READ/ READA	ILLEGAL	
	L	H	L	L	BA,CA,A10	WRIT/ WRITA	ILLEGAL	3
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	Nop → Enter idle after tRP	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

Table 3-4. Operative Commands (cont)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Command	Action	Note
Row Activating	H	X	X	X	X	DESL	Nop → Enter row active after tRCD	
	L	H	H	H	X	NOP	Nop → Enter row active after tRCD	
	L	H	H	L	X	BST	Nop → Enter row active after tRCD	
	L	H	L	H	BA,CA,A10	READ/ READA	ILLEGAL	3
	L	H	L	L	BA,CA,A10	WRIT/ WRITA	ILLEGAL	3
	L	L	H	H	BA,RA	ACT	ILLEGAL	3, 7
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write Recovering	H	X	X	X	X	DESL	Nop → Enter row active after tDPL	
	L	H	H	H	X	NOP	Nop → Enter row active after tDPL	
	L	H	H	L	X	BST	Nop → Enter row active after tDPL	
	L	H	L	H	BA,CA,A10	READ/ READA	Start read, determine AP	4
	L	H	L	L	BA,CA,A10	WRIT/ WRITA	Start read, determine AP	
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write Recovering With Auto Precharge	H	X	X	X	X	DESL	Nop → Enter precharge after tDPL	
	L	H	H	H	X	NOP	Nop → Enter precharge after tDPL	
	L	H	H	L	X	BST	Nop → Enter precharge after tDPL	
	L	H	L	H	BA,CA,A10	READ/ READA	ILLEGAL	3, 4
	L	H	L	L	BA,CA,A10	WRIT/ WRITA	ILLEGAL	3
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

Table 3-4. Operative Commands (cont)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Command	Action	Note
Refreshing	H	X	X	X	X	DESL	Nop → Enter idle after tRC	
	L	H	H	X	X	NOP/BST	Nop → Enter idle after tRC	
	L	H	L	X	X	READ/ WRITE	ILLEGAL	
	L	L	H	X	X	ACT/PRE/ PALL	ILLEGAL	
	L	L	L	X	X	REF/SELF/ MRS	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	DESL	Nop → Enter idle after tRSC	
	L	H	H	H	X	NOP	Nop → Enter idle after tRSC	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	X	X	READ/ WRITE	ILLEGAL	
	L	L	X	X	X	ACT/PRE/ PALL/REF/ SELF/MRS	ILLEGAL	

Notes:

(1) H: High level; L: Low level; X: High or low level (don't care); V: Valid data input

(2) All entries assume that CKE was active (high level) during the preceding clock cycle.

(3) Illegal to bank in specified states; function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.

(4) Must satisfy bus contention, bus turnaround, and/or write recovery requirements.

(5) If both banks are idle, and CKE is inactive (low level), the SDRAM will enter power-down mode. All input bufers except CKE will be disabled.

(6) If both banks are idle, and CKE is inactive (low level), the SDRAM will enter self-refresh mode. All input buffers except CKE will be disabled.

(7) Illegal if tRRD is not satisfied.

(8) Illegal if tRAS is not satisfied.

(9) Must satisfy burst interrupt condition.

(10) Must mask preceding data that don't satisfy tDPL.

(11) Illegal if tRCD is not satisfied.

Table 3-5. Command Truth Table for CKE

Current State	CKE n–1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Action	Note
Self-Refresh (S.R.)	H	X	X	X	X	X	X	INVALID, CLK(n–1) would exit S.R.	
	L	H	H	X	X	X	X	S.R. Recovery	2
	L	H	L	H	H	X	X	S.R. Recovery	2
	L	H	L	H	L	X	X	ILLEGAL	2
	L	H	L	L	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	Maintain S.R.	
Self-Refresh Recovery	H	H	H	X	X	X	X	Idle after tRC	
	H	H	L	H	H	X	X	Idle after tRC	
	H	H	L	H	L	X	X	ILLEGAL	
	H	H	L	L	X	X	X	ILLEGAL	
	H	L	H	X	X	X	X	ILLEGAL	
	H	L	L	H	H	X	X	ILLEGAL	
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
	L	H	X	X	X	X	X	Exit clock suspend next cycle	2
	L	L	X	X	X	X	X	Maintain clock suspend	
Power Down (P.D.)	H	X	X	X	X	X		INVALID, CLK (n–1) would exit P.D.	
	L	H	X	X	X	X	X	Exit P.D. → Idle	2
	L	L	X	X	X	X	X	Maintain power down mode	
Both Banks Idle	H	H	H	X	X	X		Refer to operations in Table 3-4	
	H	H	L	L	H	X		Refer to operations in Table 3-4	
	H	H	L	H	X	X		Refer to operations in Table 3-4	
	H	H	L	L	L	H	X	Refresh	
	H	H	L	L	L	L	Op-Code	Refer to operations in Table 3-4	
	H	L	H	X	X	X		Refer to operations in Table 3-4	
	H	L	L	H	X	X		Refer to operations in Table 3-4	
	H	L	L	L	H	X		Refer to operations in Table 3-4	
	H	L	L	L	L	H	X	Self-refresh	3
	H	L	L	L	L	L	Op-Code	Refer to operations in Table 3-4	
	L	X	X	X	X	X	X	Power-down	3

Table 3-5. Command Truth Table for CKE (cont)

Current State	CKE n–1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add	Action	Note
Any State other than listed above	H	H	X	X	X	X	X	Refer to operations in Table 3-4	
	H	L	X	X	X	X	X	Begin clock suspend next cycle	4
	L	H	X	X	X	X	X	Exit clock suspend next cycle	
	L	L	X	X	X	X	X	Maintain clock suspend	

Notes:

(1) H: High level; L: Low level; X: High or low level (don't care).

(2) CKE low-to-high transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.

(3) Power-down and self-refresh can be entered only from the Both Banks Idle state.

(4) Must be legal command as defined in Table 3-4.

Table 3-6. Command Truth Table for Two-Bank Operation

$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10	A9-A0	Action	From State	To State
H	X	X	X	X	X	X	NOP	Any	Any
L	H	H	H	X	X	X	NOP	Any	Any
L	H	H	L	X	X	X	BST	(R/W/A)0(I/A)1	A0(I/A)1
								I0(I/A)1	I0(I/A)1
								(R/W/A)1(I/A)0	A1(I/A)0
								I1(I/A)0	I1(I/A)0
L	H	L	H	H	H	CA	Read	(R/W/A)1(I/A)0	RP1(I/A)0
				H	H	CA		A1(R/W)0	RP1A0
				H	L	CA		(R/W/A)1(I/A)0	R1(I/A)0
				H	L	CA		A1(R/W)0	R1A0
				L	H	CA		(R/W/A)0(I/A)1	RP0(I/A)1
				L	H	CA		A0(R/W)1	RP0A1
				L	L	CA		(R/W/A)0(I/A)1	R0(I/A)1
				L	L	CA		A0(R/W)1	R0A1
L	H	L	L	H	H	CA	Write	(R/W/A)1(I/A)0	WP1(I/A)0
				H	H	CA		A1(R/W)0	WP1A0
				H	L	CA		(R/W/A)1(I/A)0	W1(I/A)0
				H	L	CA		A1(R/W)0	W1A0
				L	H	CA		(R/W/A)0(I/A)1	WP0(I/A)1
				L	H	CA		A0(R/W)1	WP0A1
				L	L	CA		(R/W/A)0(I/A)1	W0(I/A)1
				L	L	CA		A0(R/W)1	W0A1
L	L	H	H	H	RA		Activate Row	I1Any0	A1Any0
				L	RA			I0Any1	A0Any1

Table 3-6. Command Truth Table for Two-Bank Operation (cont)

$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10	A9-A0	Action	From State	To State
L	L	H	L	X	H	X	Precharge	(R/W/A/I)0(I/A)1	I0I1
				X	H	X		(R/W/A/I)1(I/A)0	I1I0
				H	L	X		(R/W/A/I)1(I/A)0	I1(I/A)0
				H	L	X		(I/A)1(R/W/A/I)0	I1(R/W/A/I)0
				L	L	X		(R/W/A/I)0(I/A)1	I0(I/A)1
				L	L	X		(I/A)0(R/W/A/I)1	I0(R/W/A/I)1
L	L	L	H	X	X	X	Refresh	I0I1	I0I1
L	L	L	L	Op-Code			Mode Register Access	I0I1	I0I1

Notes:

(1) Logic level abbreviations. H: High level; L: Low level; X: High or low level (don't care).

(2) Pin name abbreviation. BA: Bank address (A11)

(3) State abbreviation. I: Idle, A: Row active, R: Read with no precharge (No precharge is posted), W: Write with no precharge (No precharge is posted), RP: Read with auto precharge (Precharge is posted), WP: Write with auto precharge (Precharge is posted), Any: Any state, X0Y1 = Y1X0: Bank0 is in state "X", Bank1 is in state "Y". (XY)0Z1 = Z1(X/Y)0: Bank0 is in state "X" or "Y", Bank1 is in state "Z".

(4) If the SDRAM is in a state other than above listed in the "From State" column, the command is illegal.

(5) The states listed under "To" might not be entered on the next clock cycle. Timing restrictions apply.

3.2 Mode Register Set Command

The mode register (Figure 3-1) defines how the SDRAM operates. The mode register can be set only when both banks are in idle state. In this command, A0 through A11 are the data input pins. See Figure 3-2A. ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = Low)

During the 20 ns (tRSC) following this command, the SDRAM cannot accept any other command.

3.3 Activate Command

The SDRAM has two banks, each with 2048 rows. This command activates the bank selected by A11 (Bank Select) and a row address selected by A0 through A10. The command corresponds to a falling $\overline{RAS}$ in a conventional DRAM. See figure 3-2B. ($\overline{CS}$, $\overline{RAS}$ = Low; $\overline{CAS}$, $\overline{WE}$ = High)

3.4 Precharge Command

This command begins precharge operation of the bank selected by A11 (BS) and A10. When A10 is high, both banks are precharged, regardless of A11. When A10 is low,

only the bank selected by A11 is precharged. Low on A11 selects bank A and high selects bank B. See Figure 3-2C/D. ($\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ = Low; $\overline{CAS}$ = High**)**

After this command, the SDRAM can't accept the activate command to the precharging bank during tRP (precharge to activate command period) . The command corresponds to a conventional DRAM's rising $\overline{RAS}$.

3.5 Write Command

The write cycle starts with this command. The first column address of the write operation is set, and write data is written to the bank selected by A11. See Figure 3-2E/F. ($\overline{CS}$, $\overline{CAS}$, $\overline{WE}$ = Low; $\overline{RAS}$ = High)

When A10 is high at this command, the precharge automatically starts after the write operation for the selected bank (Write With Auto Precharge).

3.6 Read Command

The read cycle starts with this command. The first column address of the read operation is set, and the data of the bank selected by A11 is output after $\overline{CAS}$ Latency from the read command. See Figure 3-2G/H. ($\overline{CS}$, $\overline{CAS}$ = Low; $\overline{RAS}$, $\overline{WE}$ = High)

When A10 is high at this command, the precharge automatically starts after the read operation for the selected bank (Read With Auto Precharge).

3.7 CBR (Auto) Refresh Command

This command is a request to begin the CBR refresh operation. The refresh address is generated at the internal address counter and automatically counted up. Before executing CBR refresh, both banks must be in the idle (precharged) state. See Figure 3-2I. ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ = Low; $\overline{WE}$, CKE = High)

During the tRC period (from refresh command to refresh or activate command), the SDRAM cannot accept any other command. After this cycle, both banks will be in the idle (precharged) state.

3.8 Self-Refresh Entry Command

Before executing self-refresh, both banks must be in the idle (precharged) state. After execution, self-refresh operation continues while CKE remains low. When CKE goes high, the SDRAM exits the self-refresh mode. See Figure 3-2J. ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ = Low; $\overline{WE}$ = High; CKE = Low)

During self-refresh mode, refresh interval and refresh operation are performed internally, so there is no need for external control.

3.9 Burst Stop Command

This command terminates the current burst operation. See Figure 3-2K. ($\overline{CS}$, $\overline{WE}$ = Low; $\overline{RAS}$, $\overline{CAS}$ = High)

3.10 No Operation

This is not an execution command. No operations begin or terminate by this command. See Figure 3-2L/M. ($\overline{CS}$ = Low; $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = High)

Figure 3-1. Bank Select and Precharge Address Bits

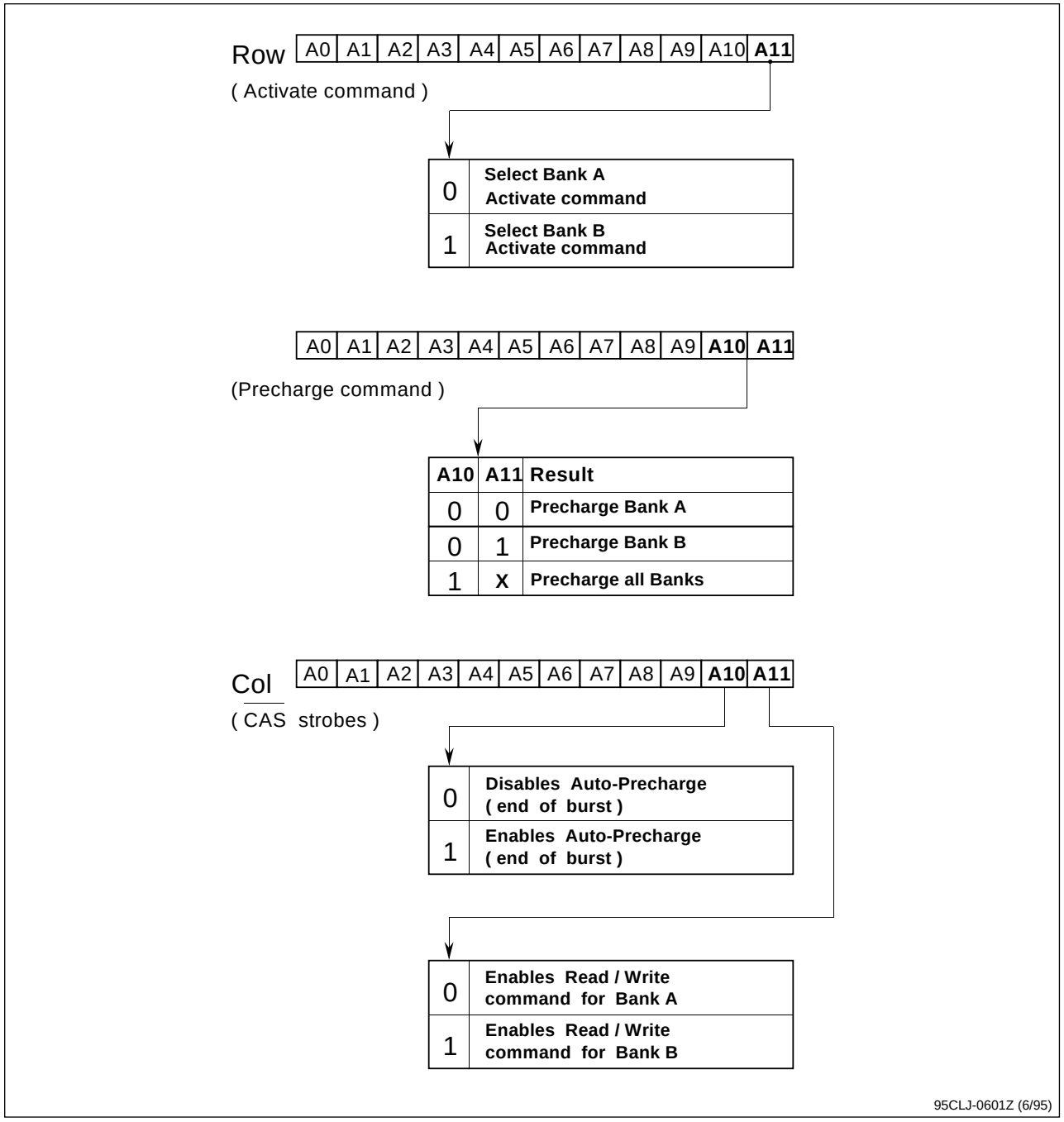


Figure 3-2. Command Timing Diagrams (1 of 3)

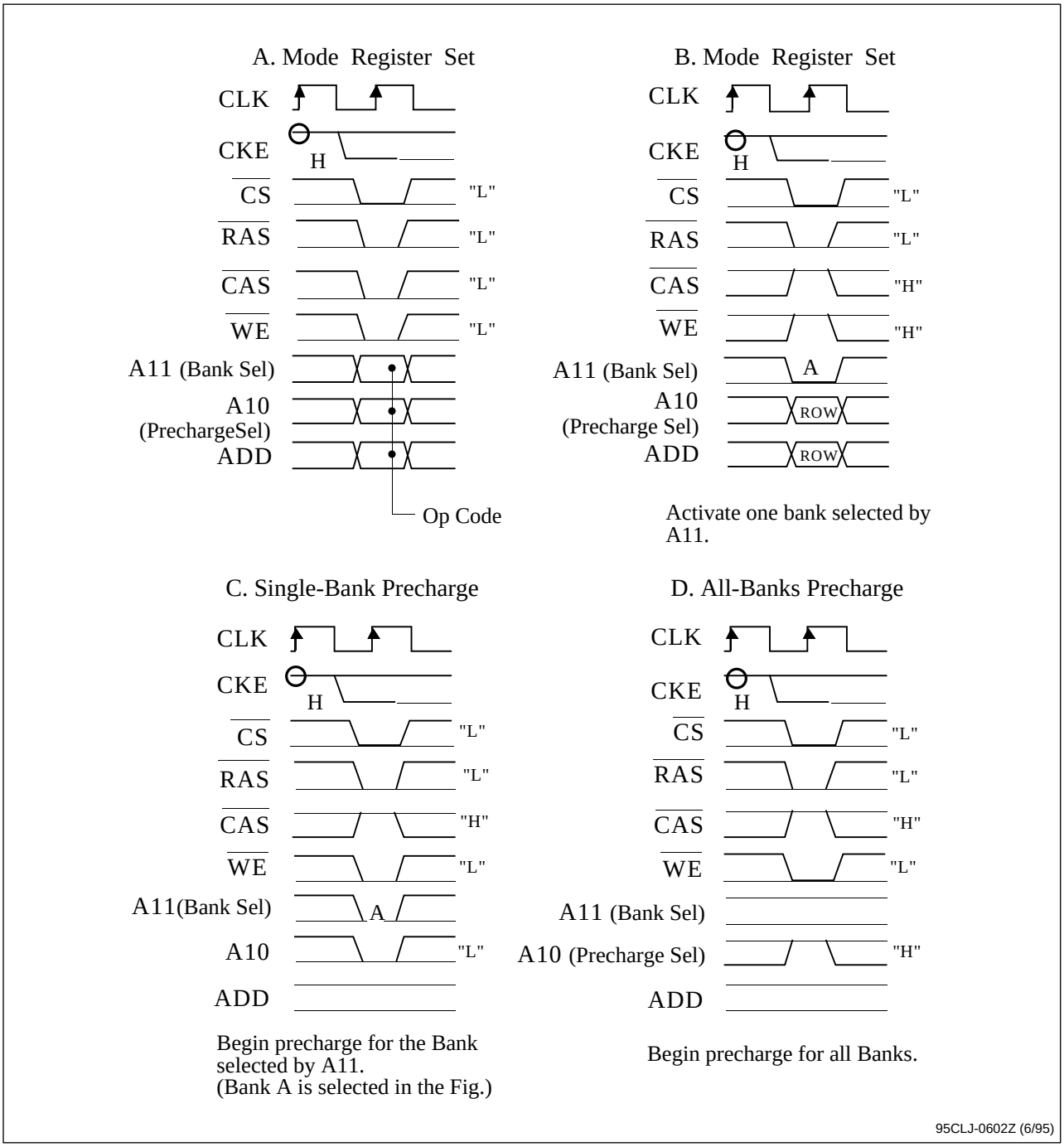


Figure 3-2. Command Timing Diagrams (2 of 3)

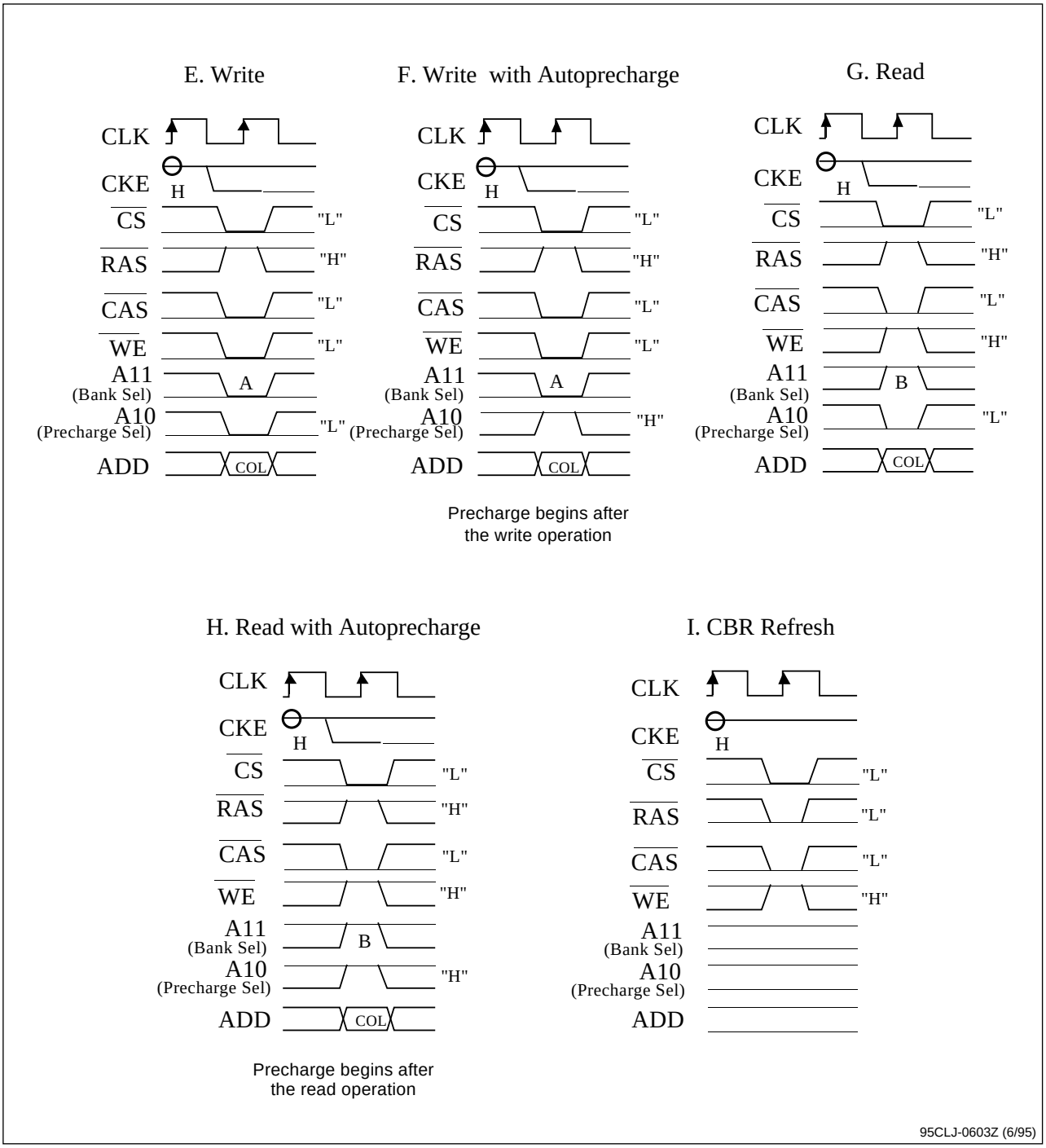
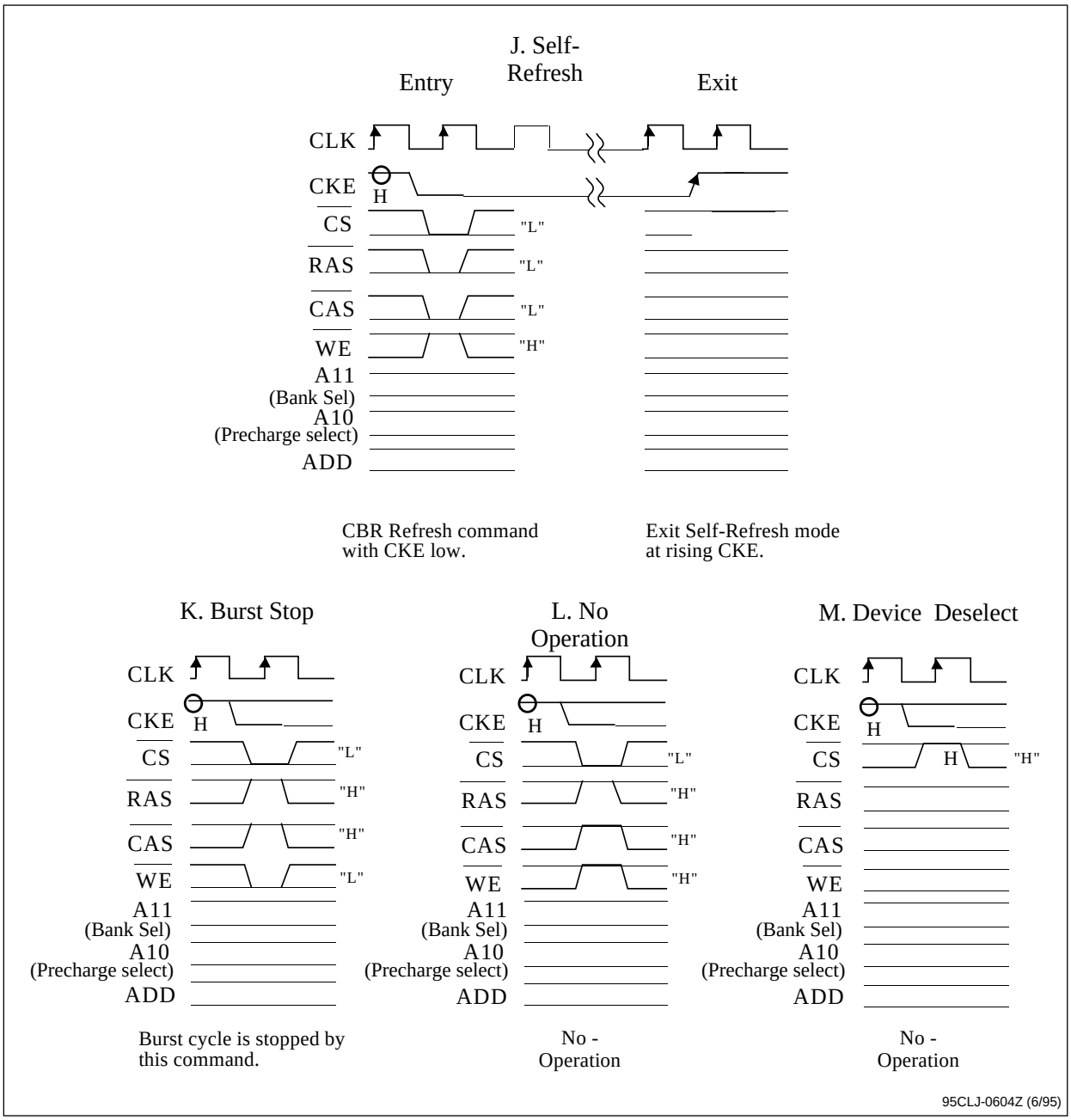


Figure 3-2. Command Timing Diagrams (3 of 3)



NEC

Basic Operating Modes 4

4.1 Read Mode

Read is executed by asserting the read command when a bank is in row active state. Table 4-1 lists ac timing parameters applicable to the Read mode. The basic flow of the read cycle follows below:

(1) Assert activate command and row address to activate the bank.

(2) Assert read command and column address.

(3) Read data corresponding to the address is output after $\overline{CAS}$ latency.

(4) Finally, assert precharge command if the bank or row address will be changed

(5) The bank will go to idle state after the tRP period.

Figure 4-1 shows the basic operating mode for the read cycle with $\overline{CAS}$ latency of two. At the rising edge of clock, T1 the activate command is asserted. After the tRCD period, the read command is asserted at T4. Then the read data is output from T7 when it is two clocks ($\overline{CAS}$ latency) after the read command.

Figure 4-2 is a timing chart for a read cycle if Auto Precharge is selected. The Read with Auto Precharge command is asserted at T4 by a high-level input to A10. The precharge command does not have to be asserted because the precharge starts automatically at T9. (Details of the Auto Precharge mode are explained in another section.)

Table 4-1. AC Parameters Applicable to Read Mode

tAC	Access time from clock	tCMS	Command setup time
tAH	Address hold time	tHZ	Data-out high-impedance time
tAS	Address setup time	tLZ	Data-out low-impedance time
tCH	Clock high-level width	tOH	Data-out hold time
tCK	Clock cycle time	tRAS	ACT to PRE command period
tCKH	CKE hold time	tRC	REF to REF/ACT command period
tCKS	CKE setup time	tRCD	Delay time ACT to READ/WRITE command
tCL	Clock low-level width	tRP	PRE to ACT command period
tCMH	Command hold time		

Figure 4-1. Read Timing

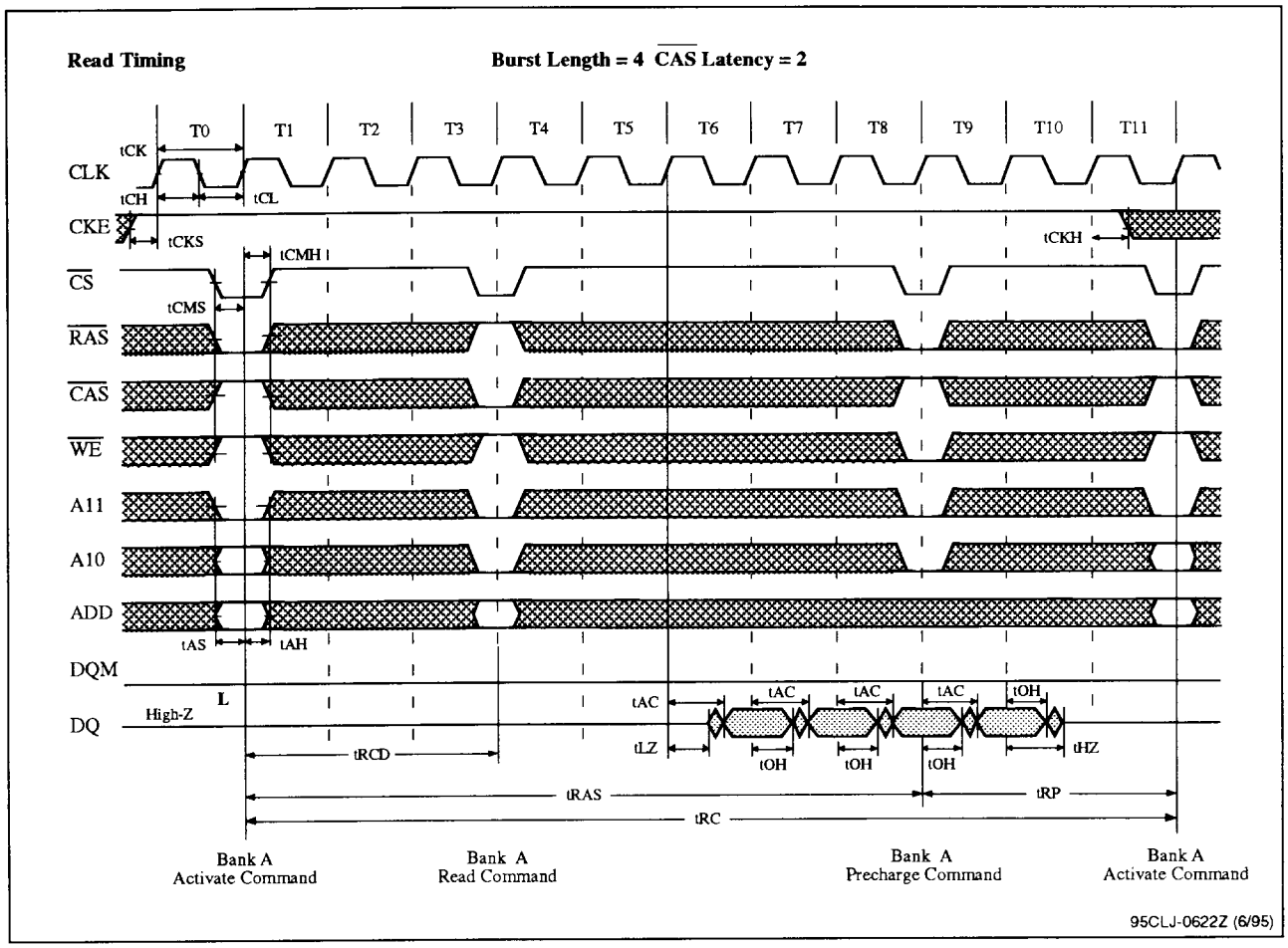
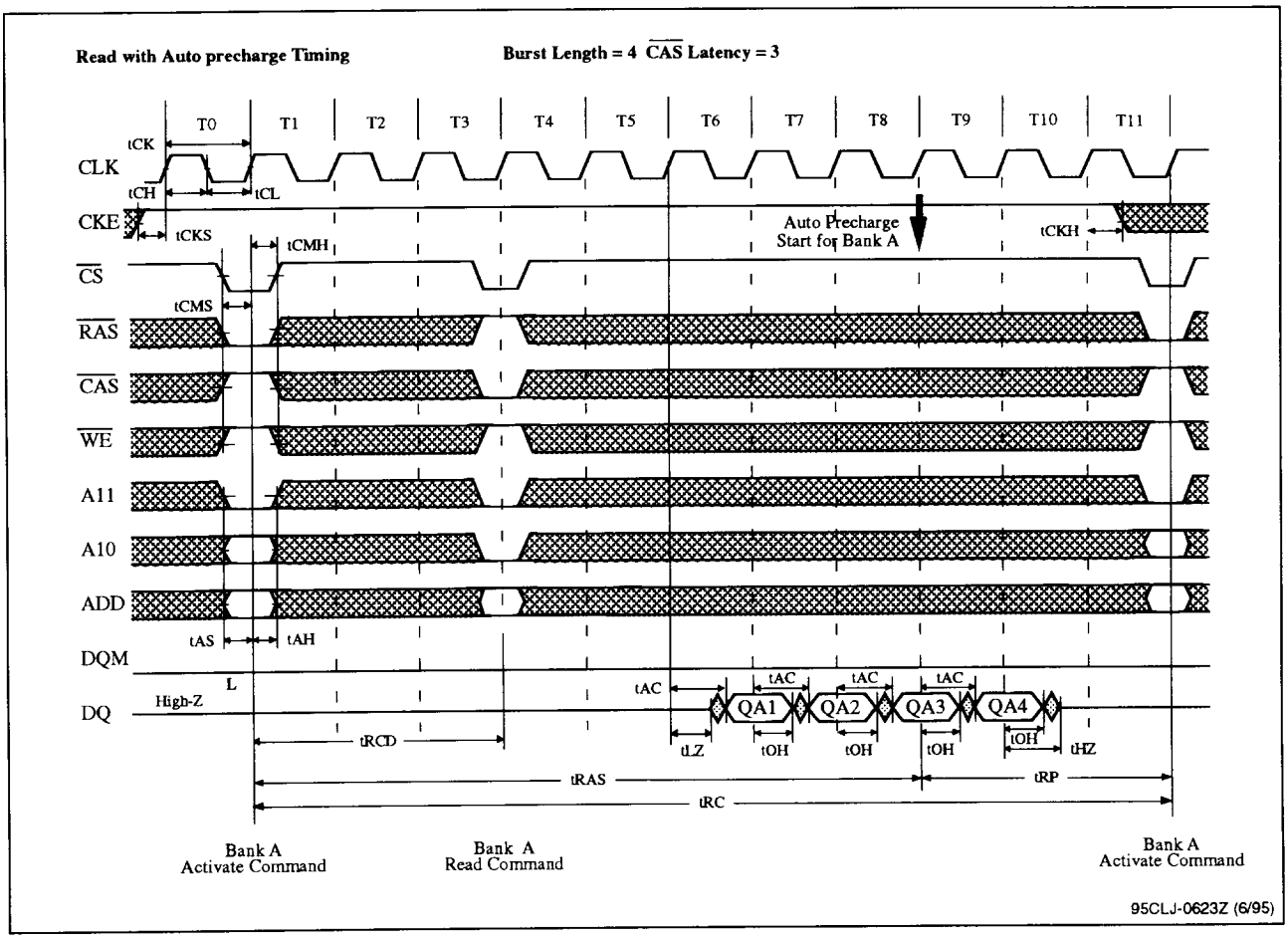


Figure 4-2. Read with Auto Precharge Timing



4.2 Write Mode

Write is executed by asserting the write command when a bank is in row active state. Table 4-2 lists ac timing parameters applicable to the Write mode; others are in Table 4-1. The basic flow of the write cycle follows below:

(1) Assert activate command and row address to activate the bank.

(2) Assert write command and column address.

(3) Input write data from the same clock as the write command (write latency is zero).

(4) Finally, asert precharge command if the bank or row address will be changed.

(5) The bank will go to idle state after the tRP period.

Figure 4-3 shows the basic operating mode for the write cycle with $\overline{CAS}$ latency of three. At the rising edge of clock T1, the activate command is asserted. After the tRCD period, the write command is asserted at T4. Then, the write data is input from

T4 when it is the same clock with the write command. The tDPL period must be satisfied to assert the precharge command for write recovery.

Figure 4-4 is a timing chart for a write cycle with Auto Precharge selected. The Write with Auto Precharge command is asserted at T4 by a high-level input to A10. The precharge command does not have to be asserted because the precharge starts automatically at T9. The tDAL period must be satisfied to assert the activate or refresh command for write recovery and precharging. (Details of the Auto Precharge mode are explained in another section).

Table 4-2. AC Parameters Applicable to Write Mode

tDAL	Last data-in to ACT/PRE command period (in Auto Precharge mode)
tDH	Data-in hold time
tDPL	Last data-in to PRE command period
tDS	Data-in setup time

Figure 4-3. Write Timing

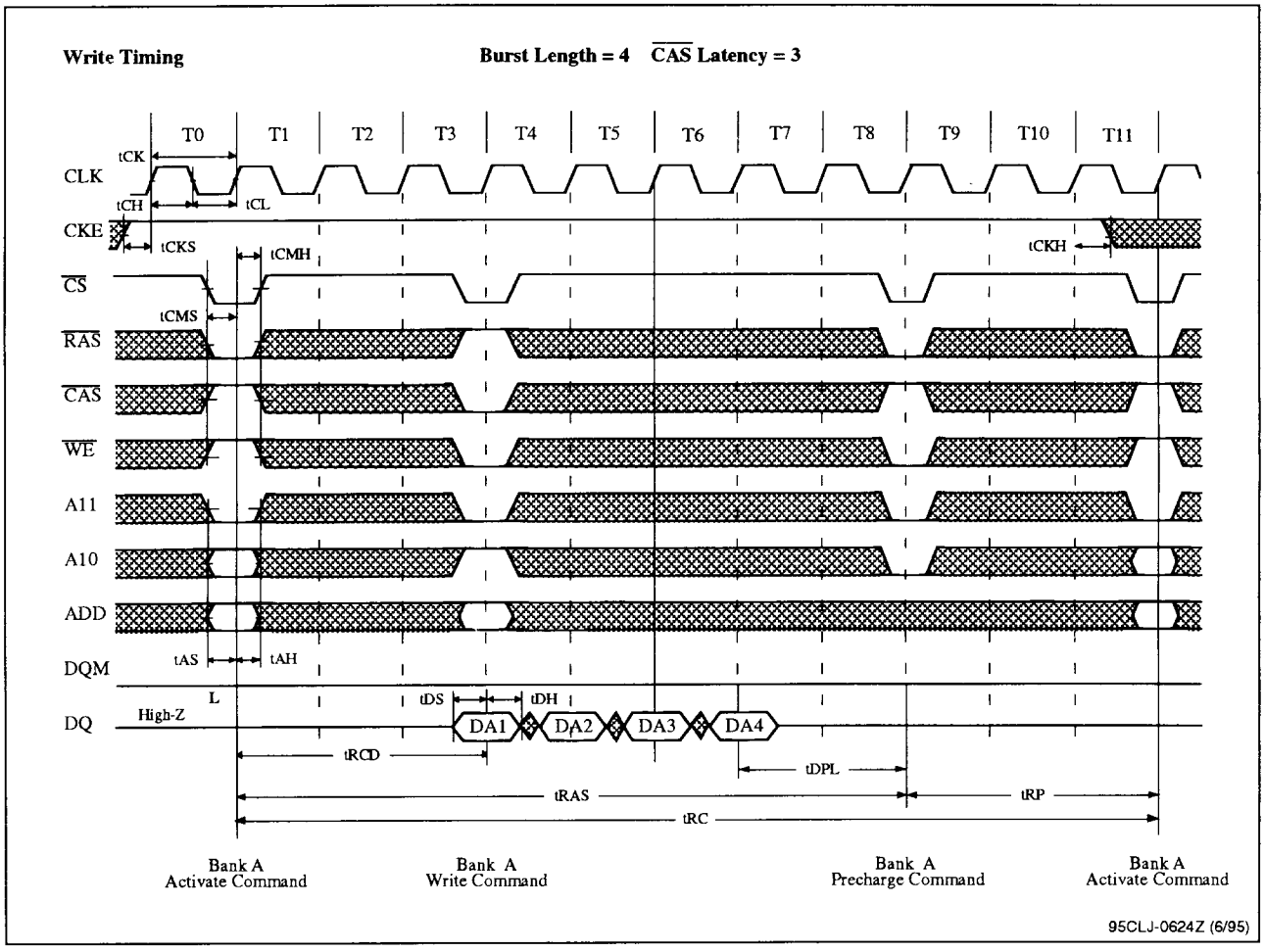
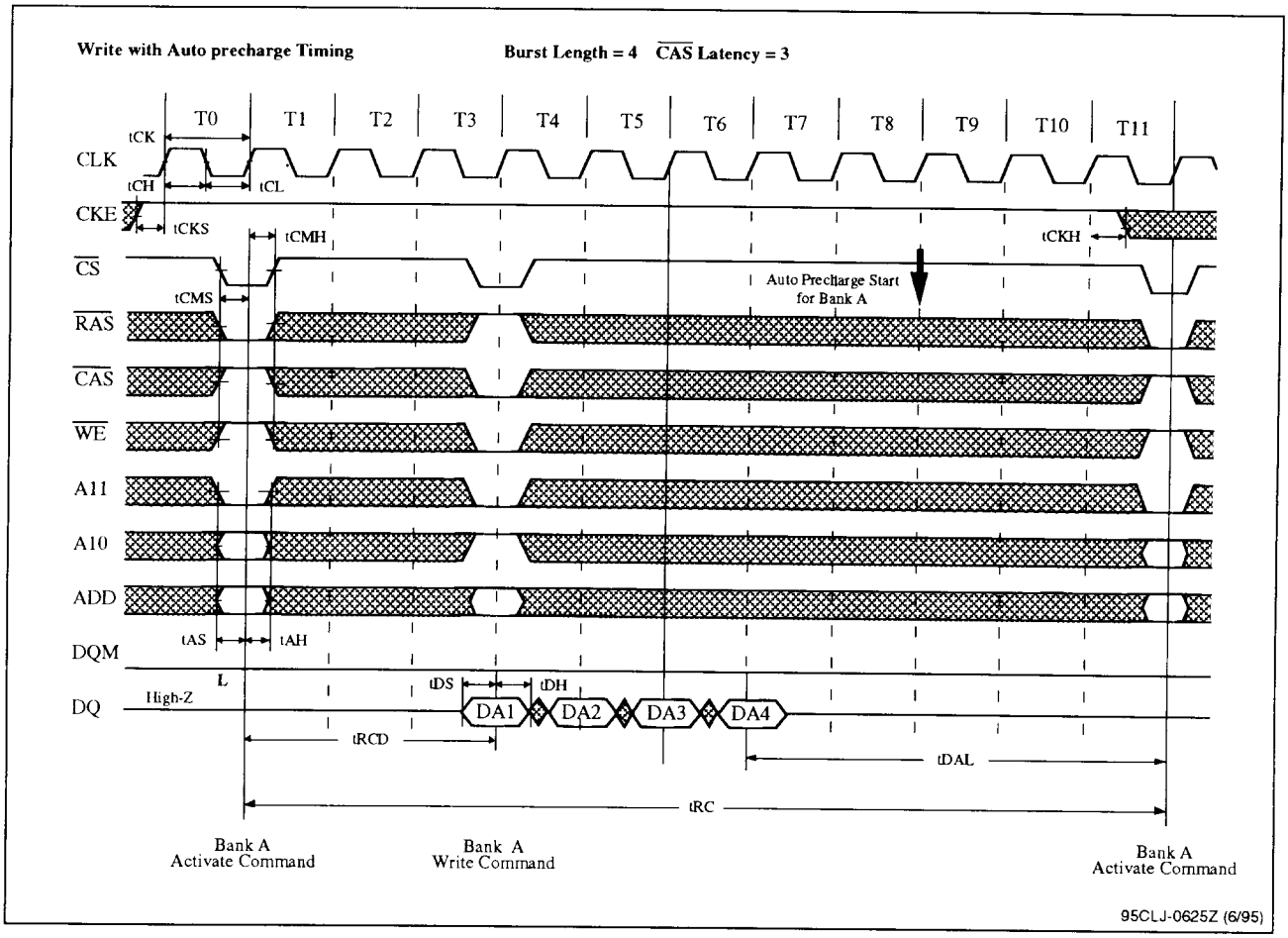


Figure 4-4. Write With Auto Precharge Timing

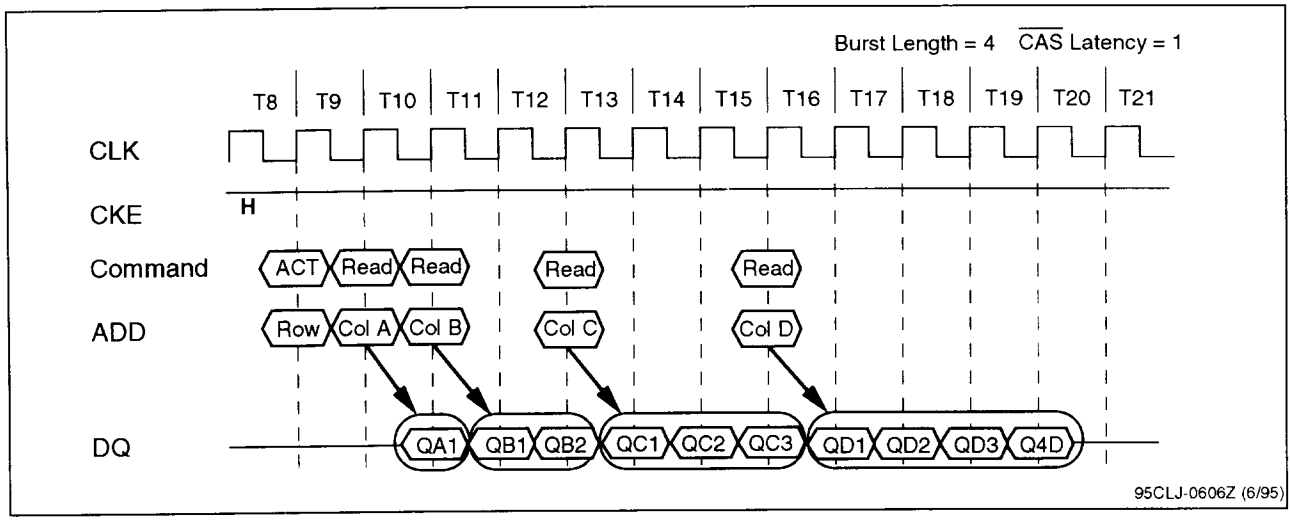


4.3 Later Command Priority

During a read cycle, if a new read command is asserted before the previous read cycle is completed, the previous read cycle is terminated and the new read command starts. The later command has priority over the previous command (Figure 4-5). By this function, the transfer word length can be changed without reprogramming the mode register.

The priority rule applies also to a write cycle and ping-pong operation (ping-pong bank).

Figure 4-5. Later Command Priority



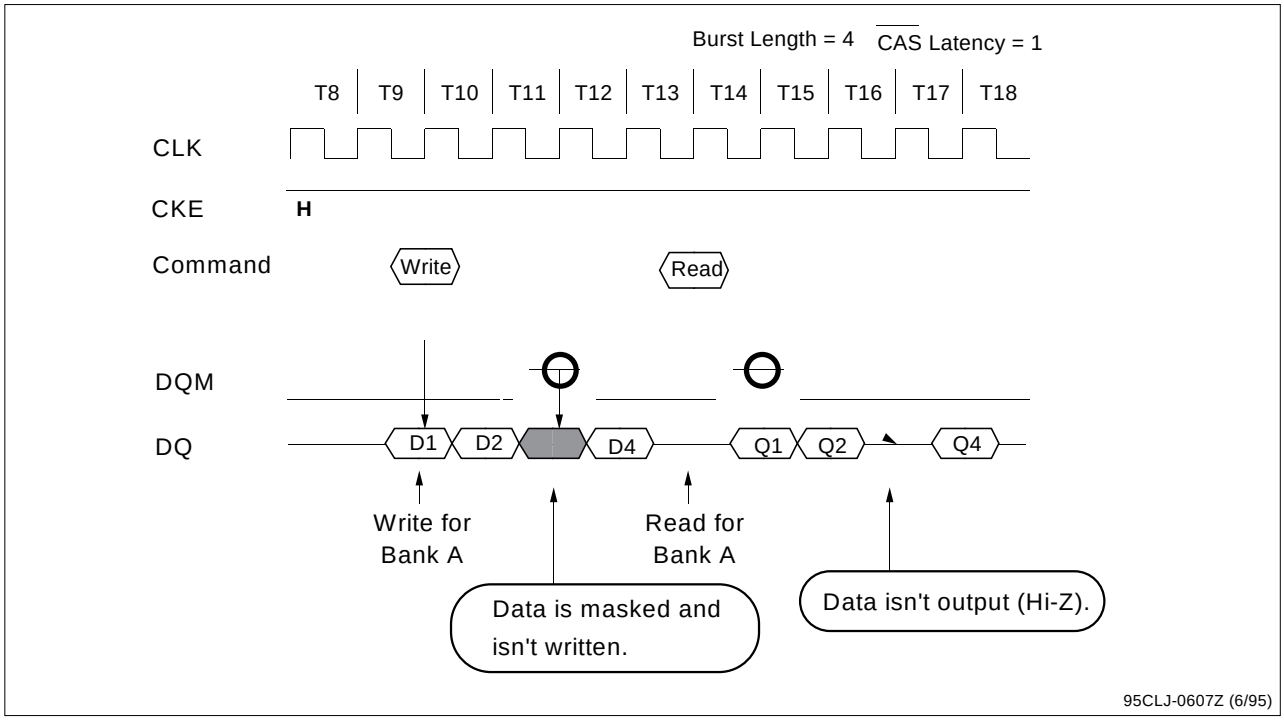
4.4 DQM Function

The DQM is defined as the data mask for both read and write. During read, the DQM performs synchronous output enable. DQM high and DQM low turn the output buffers off and on, respectively.

DQM latency for read is two clocks for all $\overline{\text{CAS}}$ latencies. DQM latency for write is zero clocks regardless of $\overline{\text{CAS}}$ latencies. (See Figure 4-6.)

During write, the DQM performs write data masking. Input data is written to the memory cell when the DQM is low, but not when the DQM is high. The upper 8 bits and lower 8 bits can be controlled independently by UDQM and LDQM in the x16 products.

Figure 4-6. DQM Function



4.5 Clock Suspension Mode

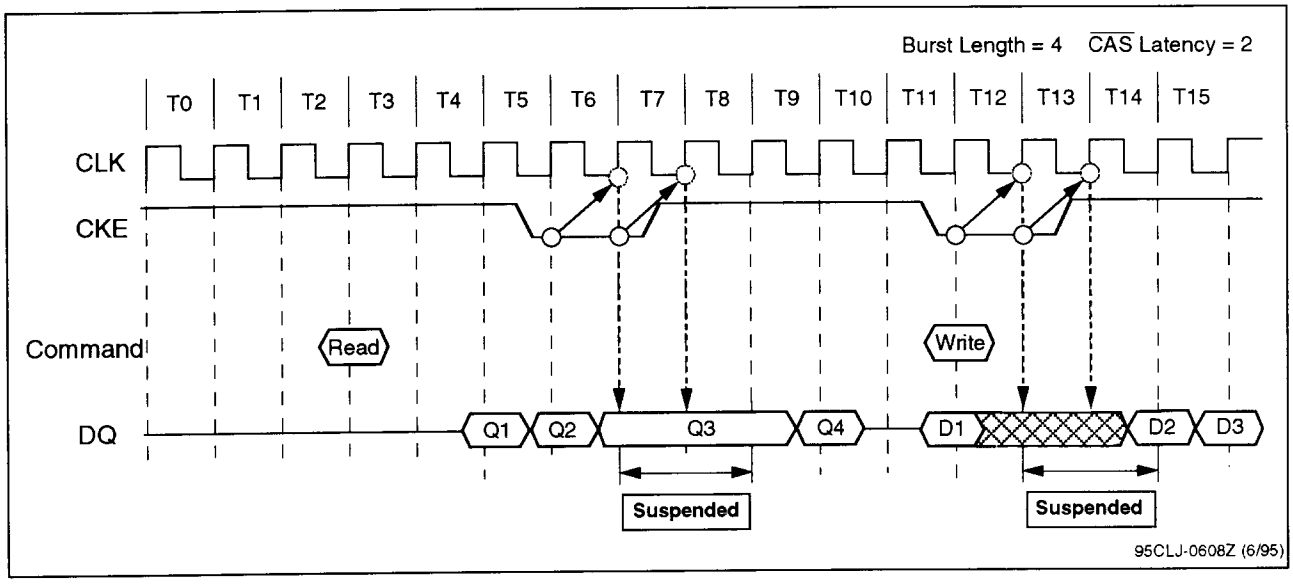
CKE as the clock enable means that external clock is transmitted to the internal blocks of the SDRAM when CKE is high, but not when CKE is low. Without external clock, the SDRAM stops synchronous operations.

In clock suspension mode, all inputs are ignored. During read, if CKE goes low, the clock suspension mode begins from the next clock. In the example of Figure 4-7, CKE goes low at T6, external T7 is not transmitted, and output data Q3 does not finish at the end of T7.

The CKE returns to high at T8, external T9 is transmitted, and Q3 finishes at the end of T9.

During write, operation is the same as read. The SDRAM enters or quits the clock suspension mode one clock after CKE goes low or high.

Figure 4-7. Clock Suspension



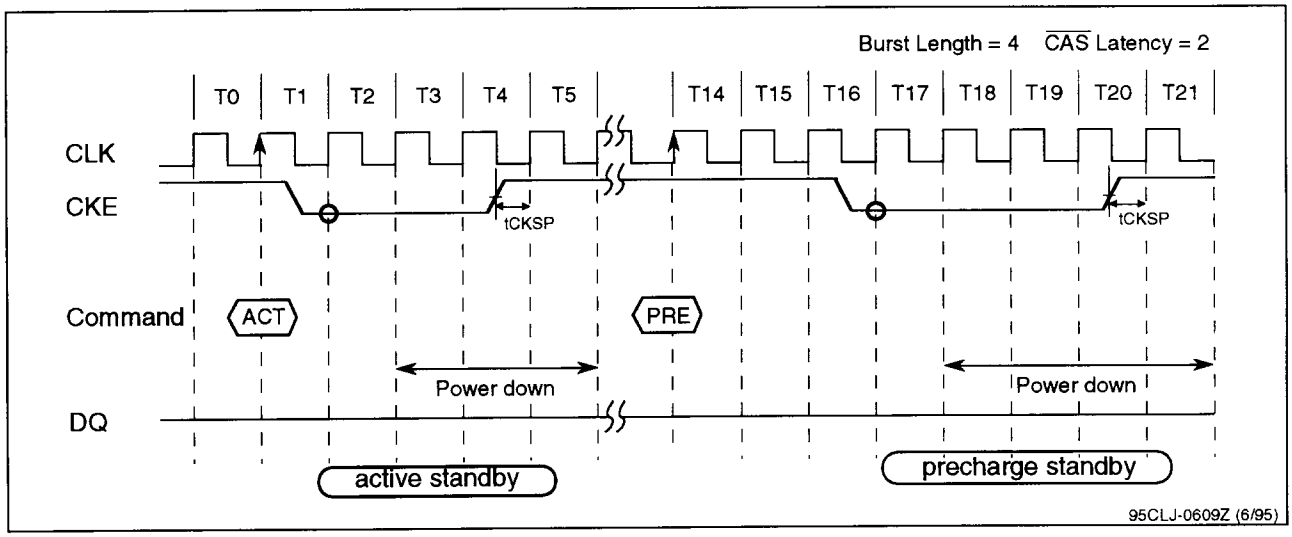
4.6 Power-Down Mode

The purpose of this mode is to reduce power by stopping the internal clock when the SDRAM is in the standby mode.

Figure 4-8 is an example of the power-down mode. The row active state is called active standby and the idle state is called precharge standby.

The timing of entering or quitting the power-down mode is the same as the clock suspension case. To quit the power-down mode, the tCKSP (CKE setup time for power-down exit) should be satisfied.

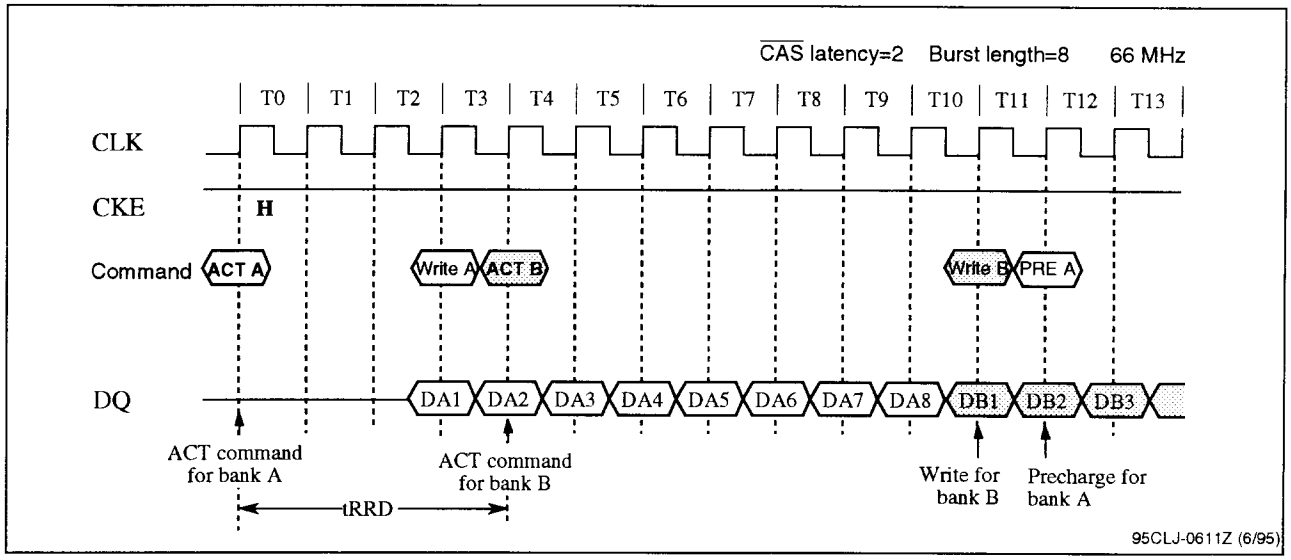
Figure 4-8. Power-Down Mode



4.7 Two-Bank Operation

Figure 4-9 is an example of banks A and B operating independently; gapless accesses, which hide a precharge time, are possible. To activate both banks, the tRRD must be satisfied between an activate command for one bank and another activate command for the other bank. The tRRD period is an asynchronous parameter so that the number of clocks depends on speed grade.

Figure 4-9. Two-Bank Operation



NEC

Timing 5

5.1 Initialization

The SDRAM is initialized in the power-on sequence according to the flow chart in Figure 5-1 and the following.

(1) To stabilize internal circuits, a 100-µs or longer pause must precede any signal toggling after power is applied.

(2) After the pause, both banks must be precharged using the Precharge command. (The Precharge All Banks command is convenient.).

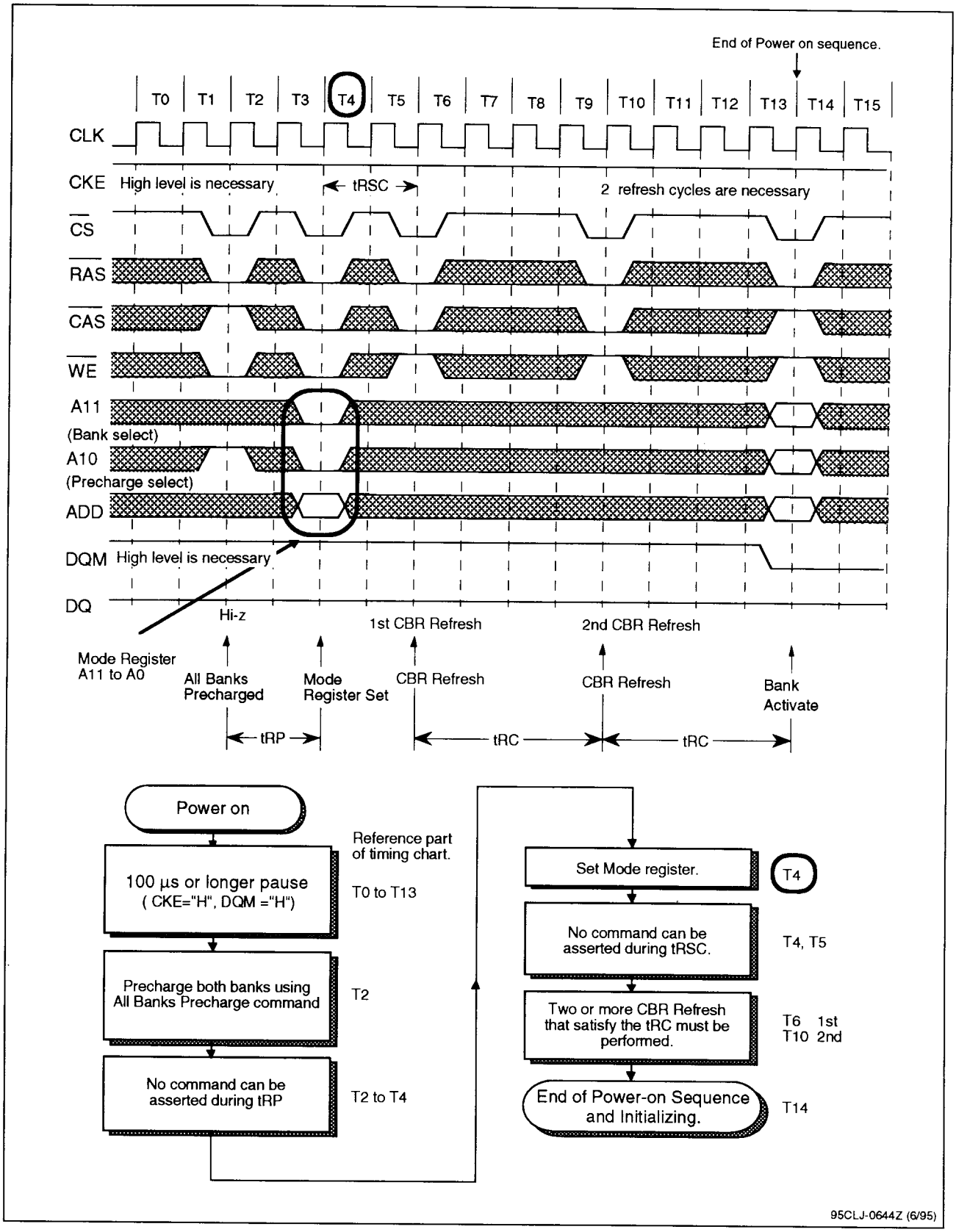
(3) Once the precharge is completed and the minimum tRP is satisfied, the mode register can be programmed. After the mode register set cycle, a tRSC (20 ns minimum) pause must be satisfied as well.

(4) Two or more CBR (Auto) Refresh cycles must be performed.

Note A: The sequence of mode register programming (3) and CBR refresh (4) above may be transposed.

Note B: CKE and DQM may be held high until the Precharge command to ensure data bus Hi-Z; otherwise, the data bus may be active

Figure 5-1. Power-On Sequence



5.2 Precharge Timing

The SDRAM has two precharge modes; one is the manual precharge mode, which is controlled by the precharge command, and the other is the auto precharge mode. This section explains the earliest timing applicable to precharge commands.

5.2.1 Manual Precharge

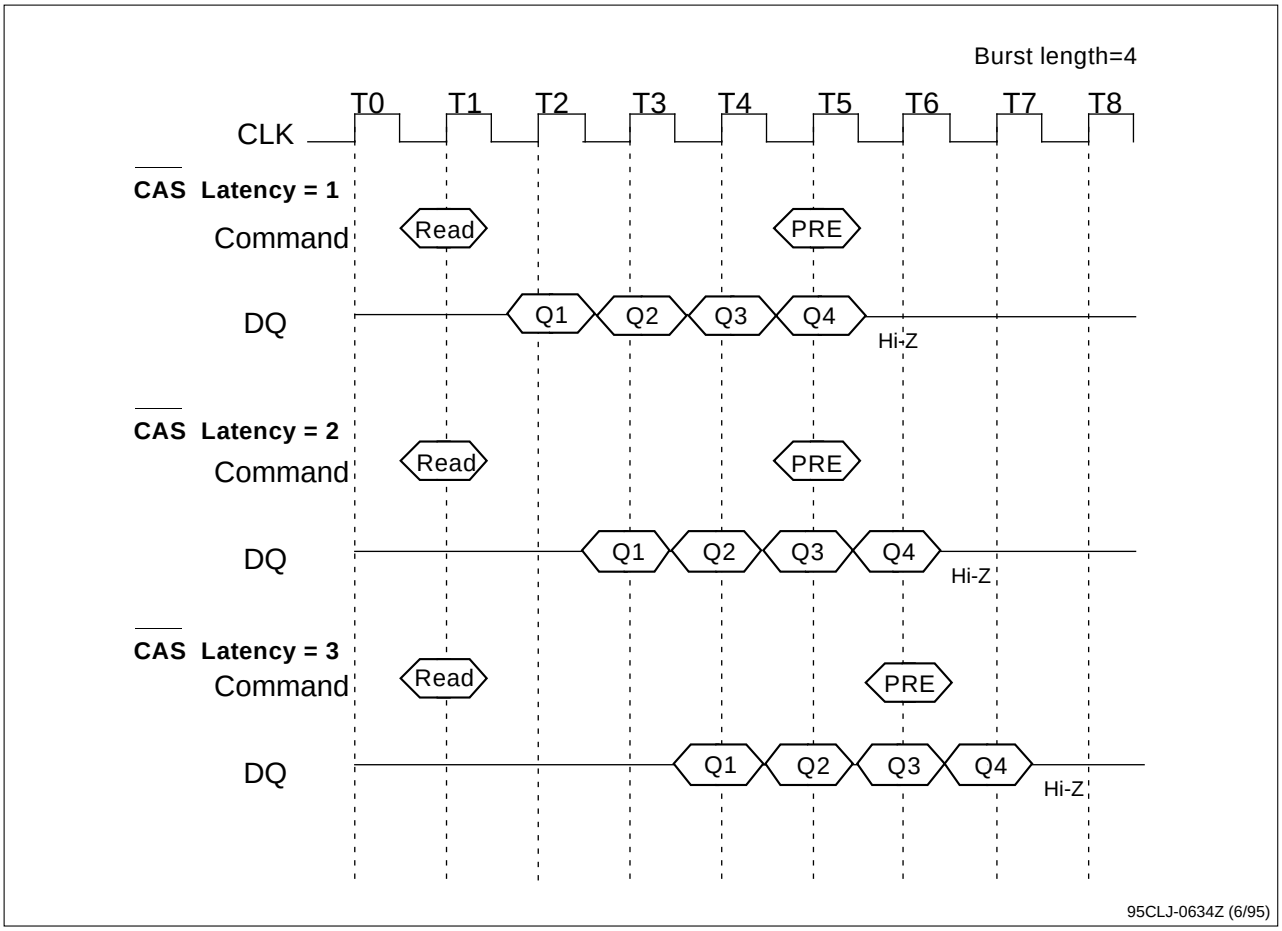
The precharge command can be asserted any time after tRAS (minimum) is satisfied. Soon after the precharge command is asserted, precharging starts and the SDRAM enters the idle state after tRP is satisfied. The same bank can be activated again from the idle state. The parameter tRP is the time to perform precharge. It is a function occurring asynchronous to system clock CLK so it is expressed in nanoseconds, not as a specific number of clocks.

(1) Read

Figure 5-2 shows the earliest in a read cycle that a precharge command can be asserted without losing any data in the burst. Depending on the $\overline{CAS}$ latency:

Latency = 1 At the same clock as the last read data.
Latency = 2 or 3 One clock earlier than the last read data.

Figure 5-2. Precharge Command Assertion During Read



(2) Write

In order to write all data to the memory cell correctly, the asynchronous parameter tDPL must be satisfied. The tDPL (min) specification defines the earliest that a precharge command can be asserted without interrupting the write operation. This translates to the device's "write recovery time."

When DQM is used to mask invalid data, the reference is from the last unmasked write data.

Figure 5-3 shows the earliest in a write cycle that a precharge command can be asserted. Minimum clocks are shown for each grade part operated at minimum clock cycles according to $\overline{CAS}$ latency.

(3) Summary

In summary, the precharge command can be asserted relative to a reference clock that indicates the last data word is valid. In Table 5-1, minus in the Read column means clocks before the reference; plus in the Write column means time after the reference.

Figure 5-3. Precharge Command Assertion During Write

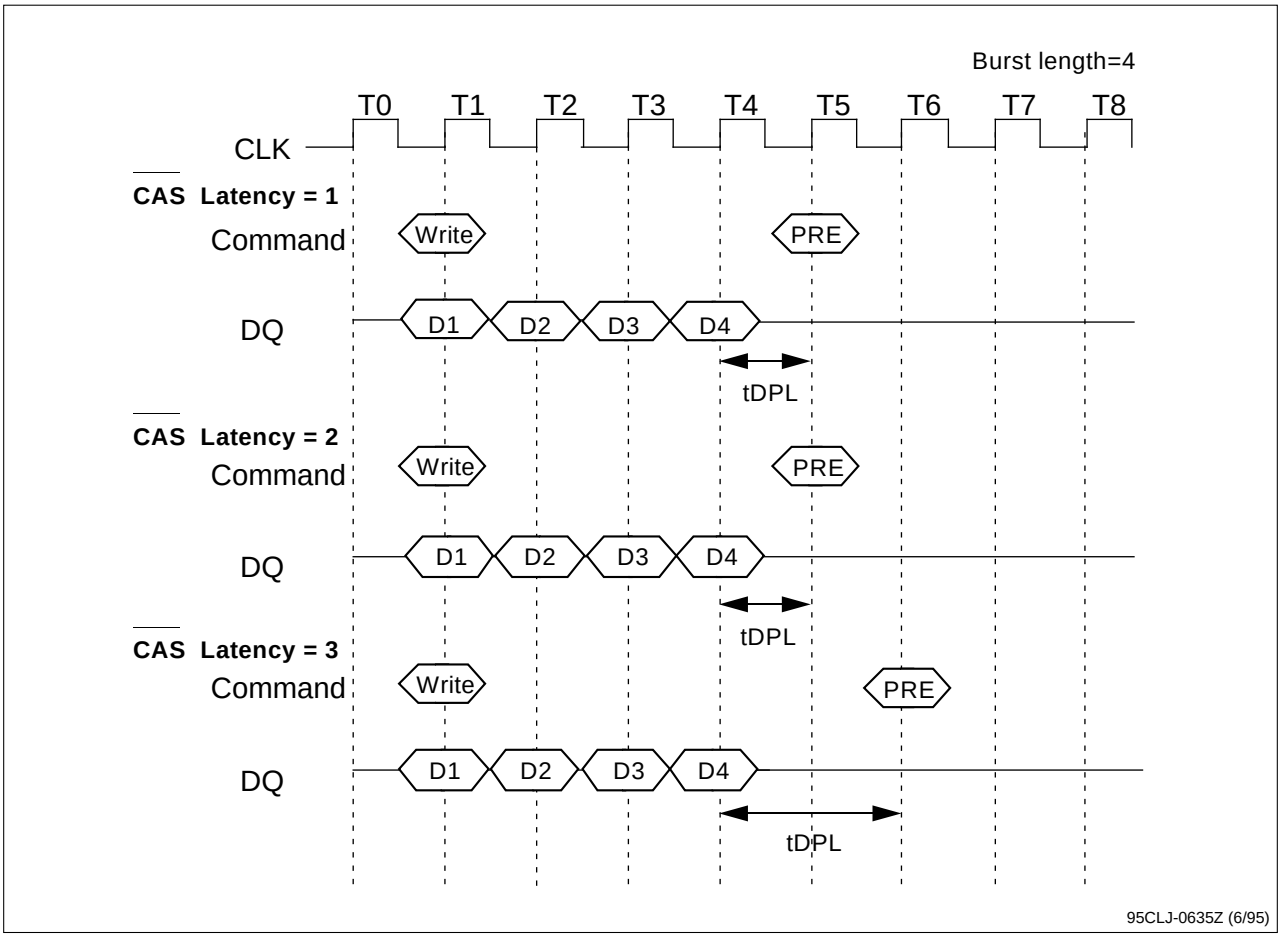


Table 5-1. Earliest Timing a Precharge Command Can Be Asserted

$\overline{\text{CAS}}$ Latency	Read	Write
1	0	+tDPL (min)
2	–1	+tDPL (min)
3	–1	+tDPL (min)

5.2.2 Auto Precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. If A10 is high, auto precharge is selected and precharge begins automatically after the read or write.

Once auto precharge begins, the SDRAM will go to the idle state, and an activate command to the bank can be asserted after tRP is satisfied.

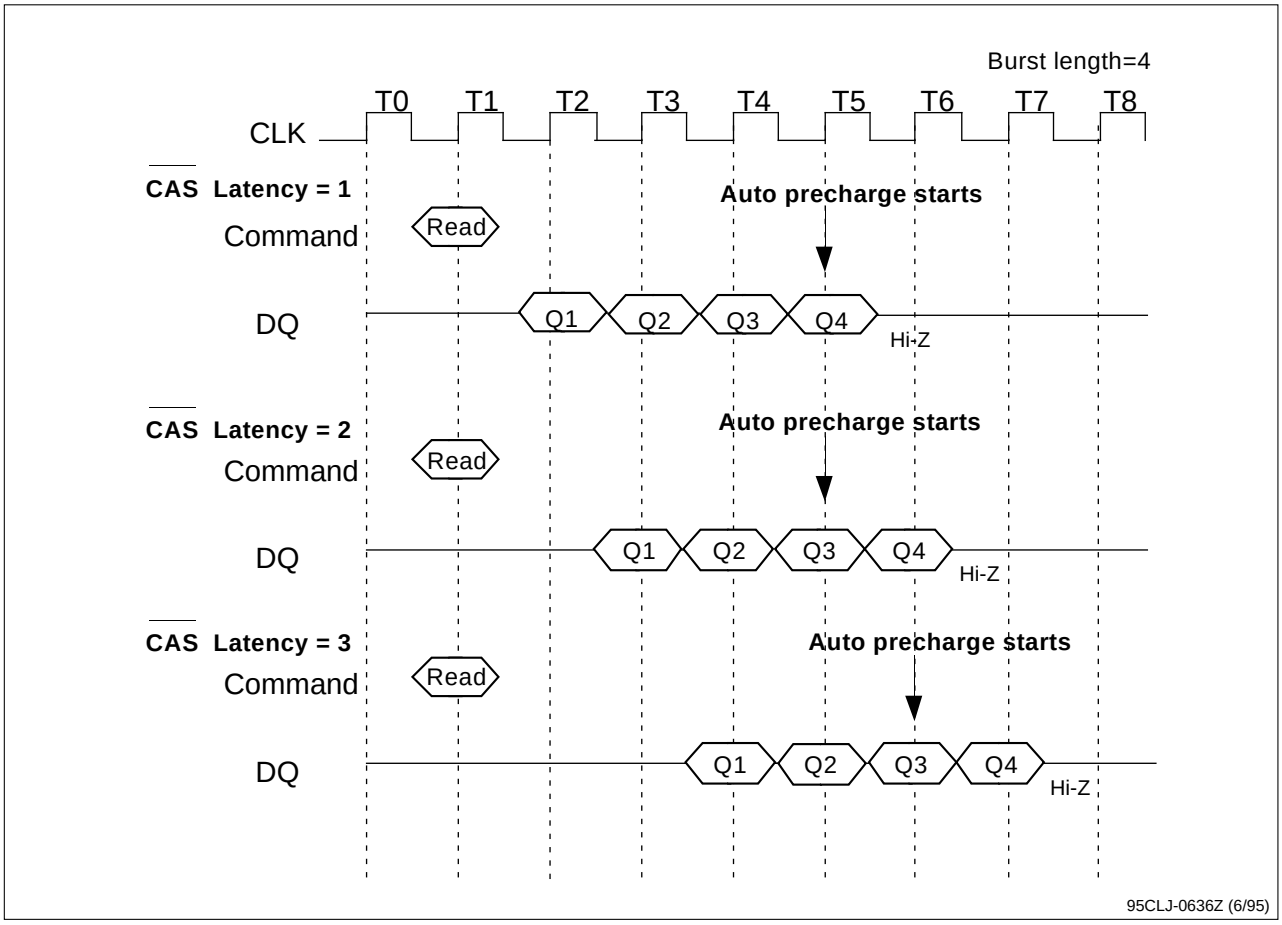
(1) Read

When using auto precharge in a read cycle, knowing when precharge begins is important because the next activate command to the bank being precharged cannot be executed until the precharge operation finishes.

Figure 5-4 shows when precharge begins in a read cycle if auto precharge is selected, depending on the $\overline{CAS}$ latency.

Latency = 1 At the same clock as the last read data.
Latency = 2 or 3 One clock earlier than the last read data.

Figure 5-4. Auto Precharge Start Timing During Read



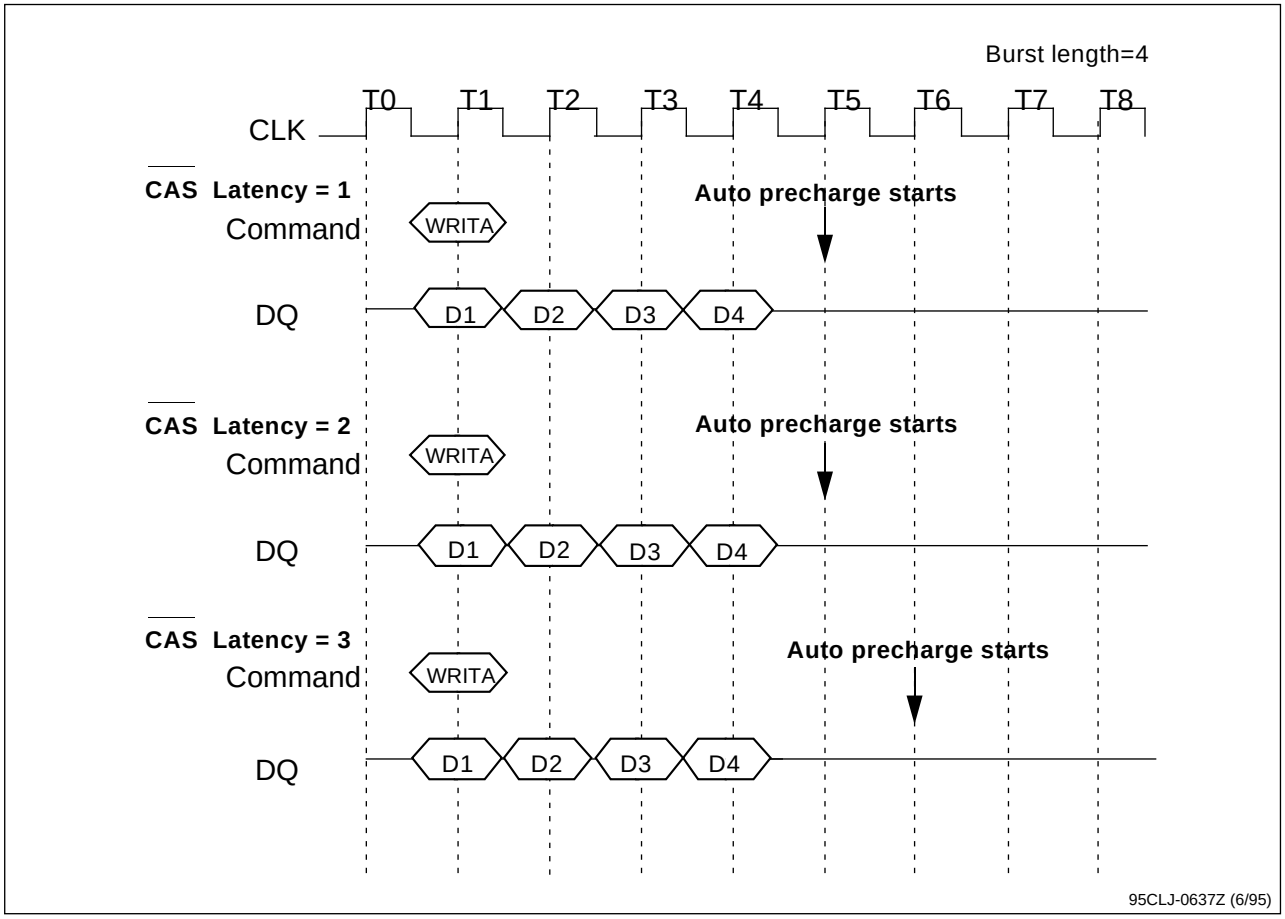
(2) Write

When using auto precharge in a write cycle, tDAL must be satisfied to assert the next activate command to the bank being precharged. The tDPL includes write recovery time and precharge time.

Figure 5-5 shows when precharge begins in a write cycle if auto precharge is selected, depending on the $\overline{CAS}$ latency.

Latency = 1 or 2 One clock after the last write data.
Latency = 3 Two clocks after the last write data.

Figure 5-5. Auto Precharge Start Timing During Write



(3) Summary

In summary, auto precharge begins relative to a reference clock that indicates the last data word is valid. In Table 5-2, minus in the Read column means clocks before the reference; plus in the Write column means clocks after the reference.

Table 5-2. Precharge Beginning Timing in Auto Precharge Mode

$\overline{\text{CAS}}$ Latency	Read	Write
1	0	+1
2	–1	+1
3	–1	+2

When tRAS is not satisfied, the precharge does not start at the timing above. The precharge will start when tRAS is satisfied.

5.3 Mode Register Programming

The mode register (Figure 5-6) is programmed by the Mode Register Set command using address bits A11 through A0 as data inputs. The register retains data until it is reprogrammed or the device loses power.

The mode register has four fields:

Burst length	A2 through A0
Wrap type	A3
$\overline{\text{CAS}}$ latency	A6 through A4
Options	A11 through A7

After mode register programming, no command can be asserted for at least 20 ns (tRSC).

Figure 5-7 is an example of Mode Register programming and read / write operation. In this example, $\overline{\text{CAS}}$ latency of 2, burst length of 2, and either wrap type are programmed.

Figure 5-6. Mode Register

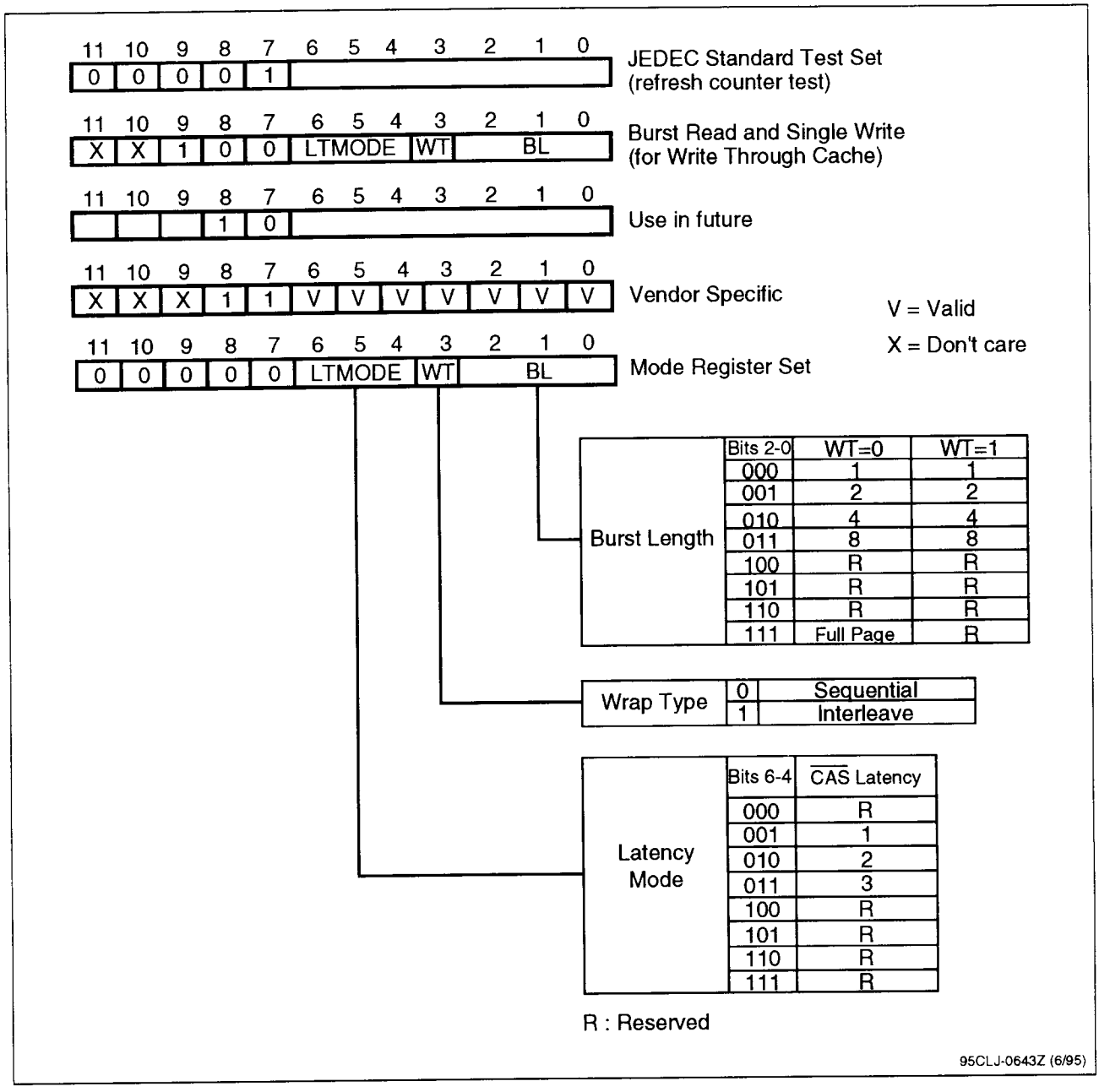
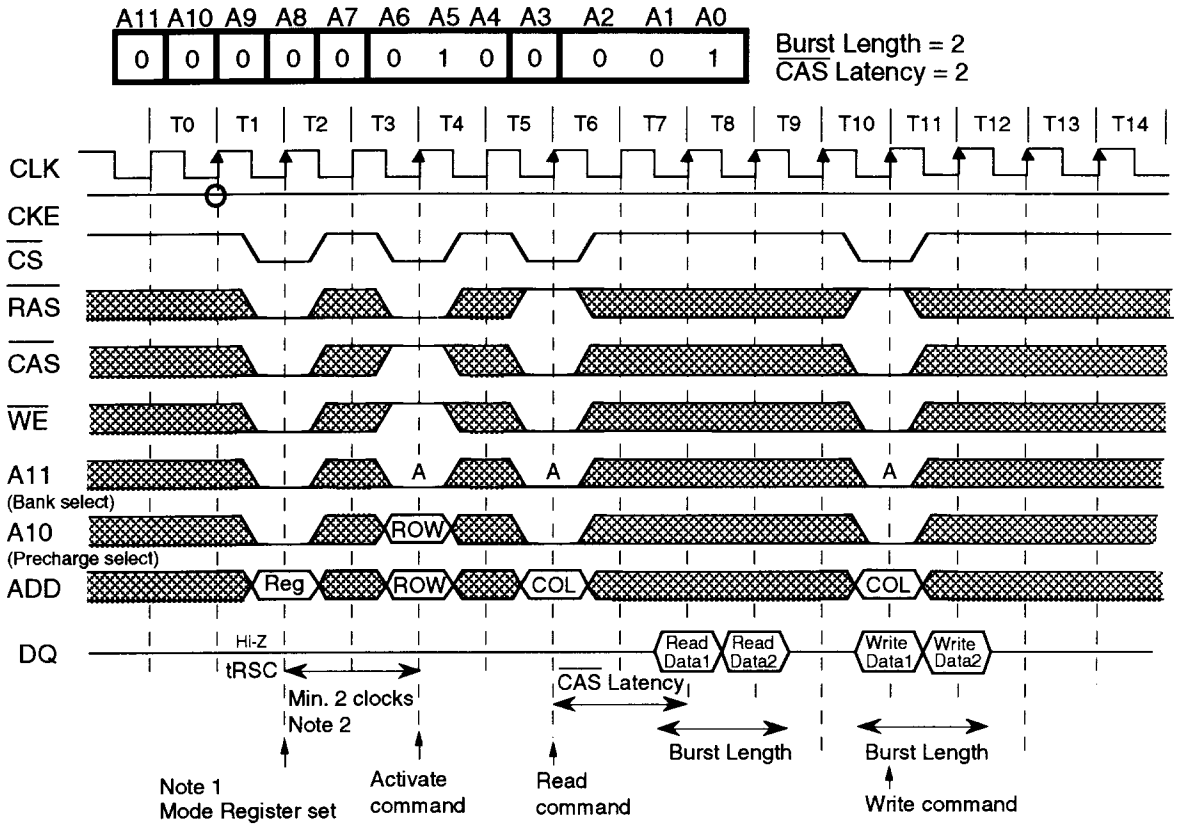


Figure 5-7. Mode Register Set Example



Note:

1. Both banks must be precharged (idle state) before the Mode Register set.
2. No command can be issued during this period, minimum 20 ns.

95CLJ-0645Z (6/95)

5.4 $\overline{\text{CAS}}$ Latency

Of the parameters being set, $\overline{\text{CAS}}$ latency is the most critical. It tells the device how many clocks must elapse before data will be available. The NEC SDRAM is capable of reconfiguring its internal architecture based on the value of $\overline{\text{CAS}}$ latency. The value is determined by the clock frequency and the speed grade of the device.

5.4.1 Burst Length

Burst length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus becomes high impedance.

The burst length is programmable as 1, 2, 4, 8, or full page. Full-page burst is only for sequential addressing, with the length being 1024 (4M x 4), 512 (2M x 8), or 256 (1M x 16).

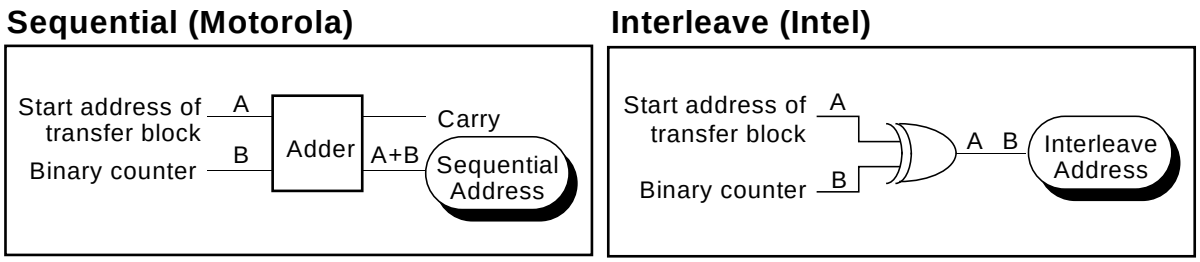
If the burst continues at the end column address (boundary), the burst goes back to the first address of the same row.

5.4.2 Wrap Type

The wrap type (burst sequence) specifies the order in which the burst data will be addressed . This order is programmable as either “Sequential” or “Interleave.” The method chosen depends on the type of CPU in the system.

Some microprocessor cache systems are optimized for sequential addressing and others for interleaved addressing. Both sequences support bursts of 1, 2, 4, and 8 words; the sequential sequence also supports the full-page length. See Figure 5-8.

Figure 5-8. Wrap Types



Burst Length = 8

Order	Start Address of Transfer Block.	Binary Counter	Sequential Addressing	Interleave Addressing
	Binary (Decimal)			
↓	**010 (2)**	**000 (0)**	**010 (2)**	**010 (2)**
	010 (2)	**001 (1)**	**011 (3)**	**011 (3)**
	010 (2)	**010 (2)**	**100 (4)**	**000 (0)**
	010 (2)	**011 (3)**	**101 (5)**	**001 (1)**
	010 (2)	**100 (4)**	**110 (6)**	**110 (6)**
	010 (2)	**101 (5)**	**111 (7)**	**111 (7)**
	010 (2)	**110 (6)**	**000 (0)**	**100 (4)**
	010 (2)	**111 (7)**	**001 (1)**	**101 (5)**

95CLJ-0642Z (6/95)

5.5 Refresh

The SDRAM has the same need for refreshing as conventional DRAMs. The refresh cycle of the SDRAM is 2048/32 ms, meaning that 2048 refresh cycles are required during each 32-ms interval. This requirement should be strictly observed; otherwise, data stored in the memory may by destroyed. Refresh cycles can be executed in two ways.

(1) Distributed refresh: Refresh is performed at intervals. For the SDRAM, refresh cycles may be executed every 15.6 µs (32 ms divided by 2048).

(2) Burst refresh: Refresh cycles are executed in succession.

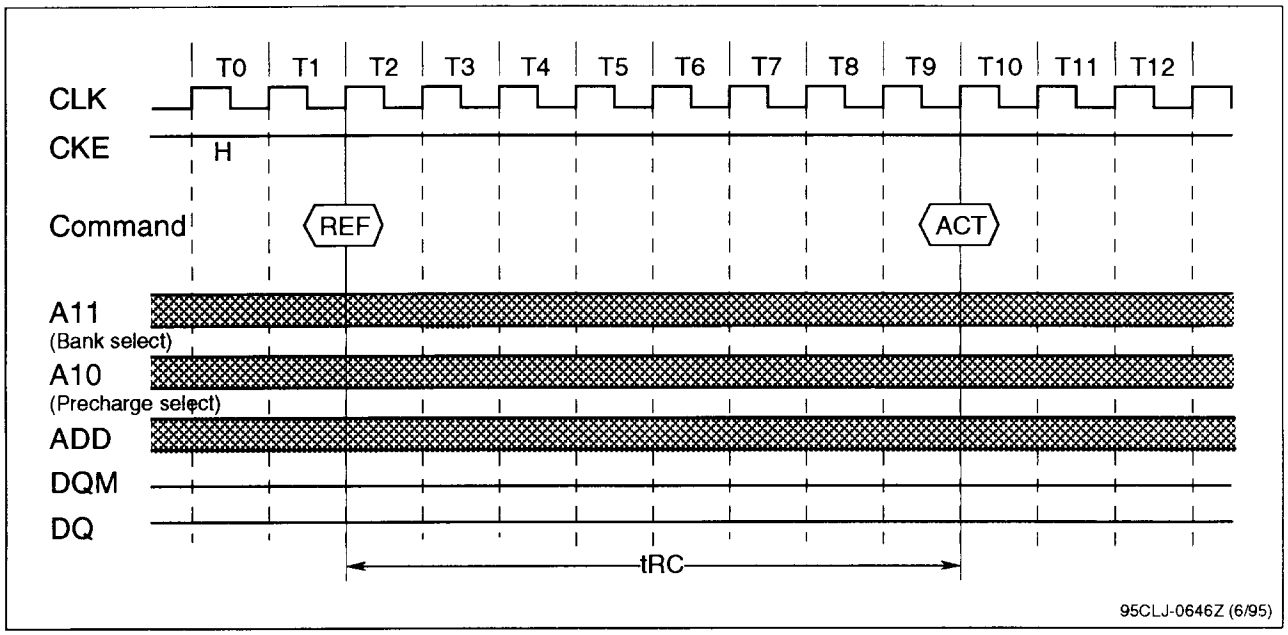
5.5.1 CBR Refresh

The CBR refresh (also called auto-refresh) is generally used in nomal read or write mode. The refresh cycle is executed with a CBR Refresh command assertion from the idle state. An internal counter automatically generates 2048 different addresses.

Once a refresh operation is executed, the idle state is resumed. A tRC period is required before another command is asserted (Figure 5-9).

Note: Refresh operation can be completed in read or write cycles by changing all addresses during a 32-ms interval (tREF).

Figure 5-9. CBR Refresh Timing



5.5.2 Self-Refresh

Self-refresh is generally used for power reduction. It is similar to CBR refresh except CKE is low. Self-refresh mode continues while CKE remains low.

To exit self-refresh, there are two options:

(1) CKE high with DESEL command ($\overline{CS}$ = high)

(2) CKE high with NOP command ($\overline{CS}$ = low; $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = high)

In addition, CKE must stay high with the DESEL or NOP command asserted for the tRC period; no other command can be asserted for the period (Figure 5-10).

Note: When burst refresh and self-refresh are used in combination, perform CBR refresh 2048 times within an 8-ms interval just before and after exiting self-refresh (Figure 5-11).

Figure 5-10. Self-Refresh Timing

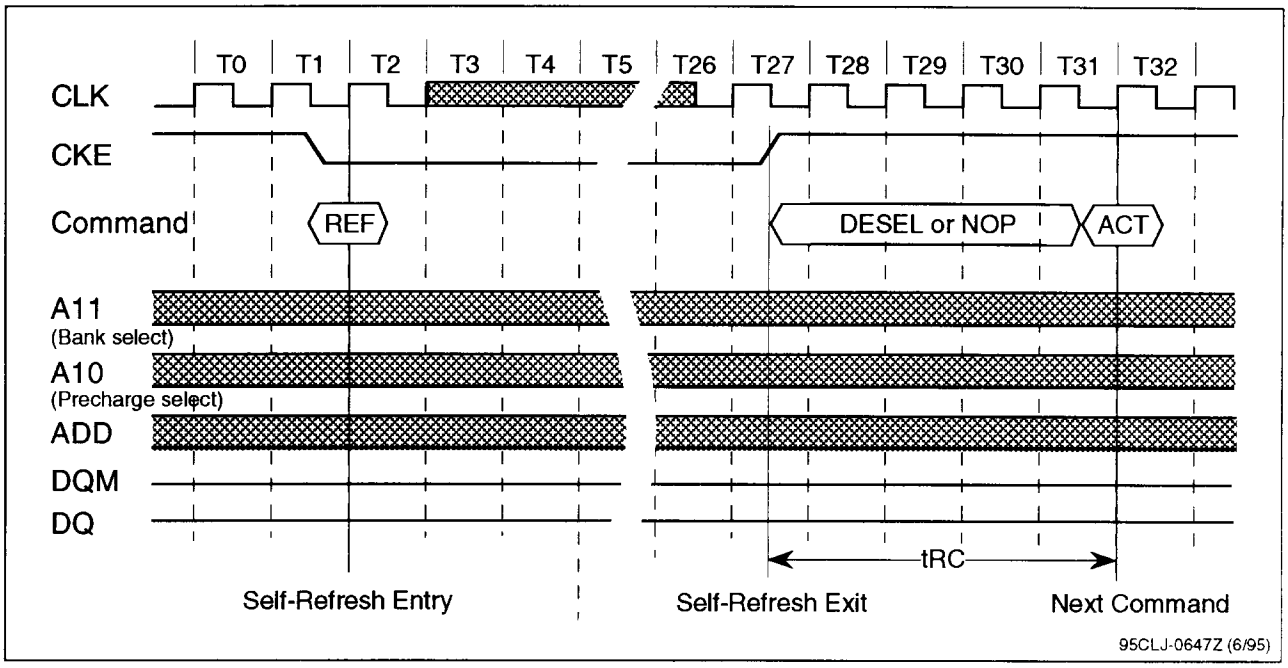
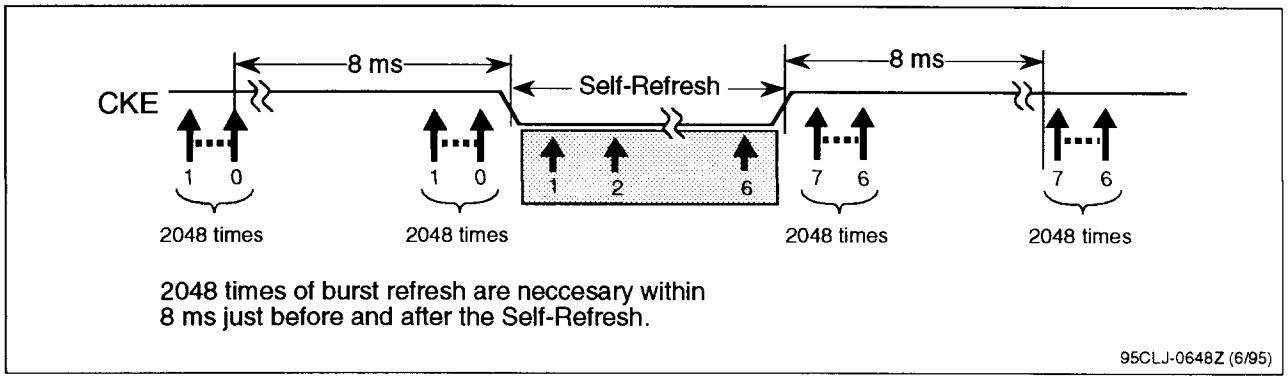


Figure 5-11. Burst Refresh Timing



Burst Operation 6

6.1 Burst Termination

There are two methods to terminate a burst operation other than a read or write command. One is the burst stop command and the other is the precharge command.

6.1.1 Burst Stop Command

During a read cycle, when the burst stop command is asserted, the burst read data is terminated, and the data bus goes to high impedance after the $\overline{\text{CAS}}$ latency from the burst stop command (Figure 6-1).

During a write cycle, when the burst stop command is asserted, the burst read data is terminated, and the data bus goes to high impedance at the same clock with the burst stop command (Figure 6-2).

Figure 6-1. Burst Stop Command for Read

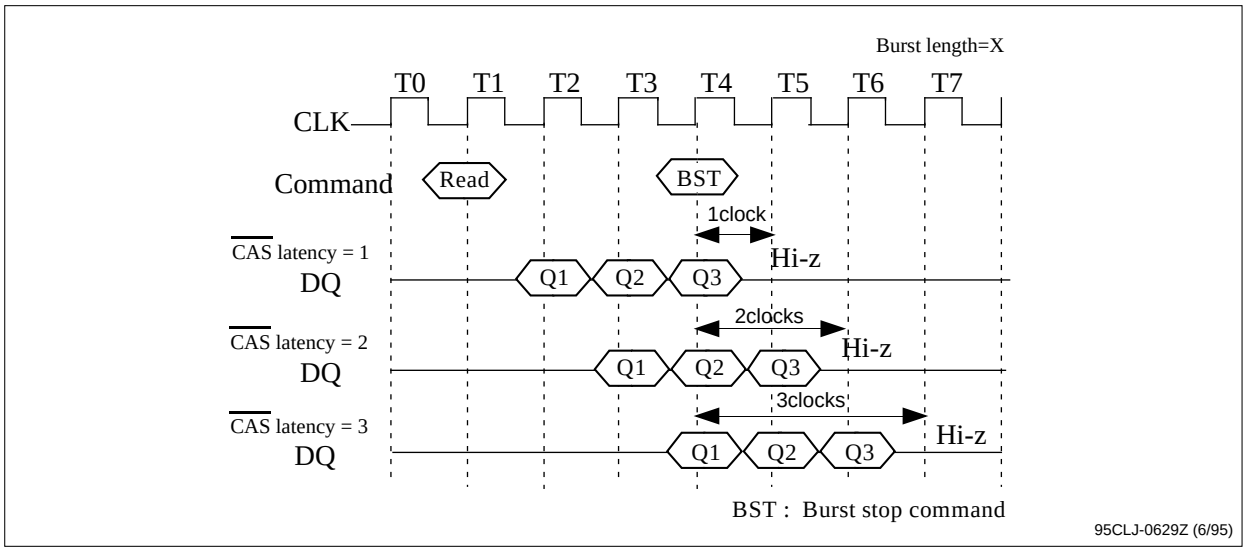
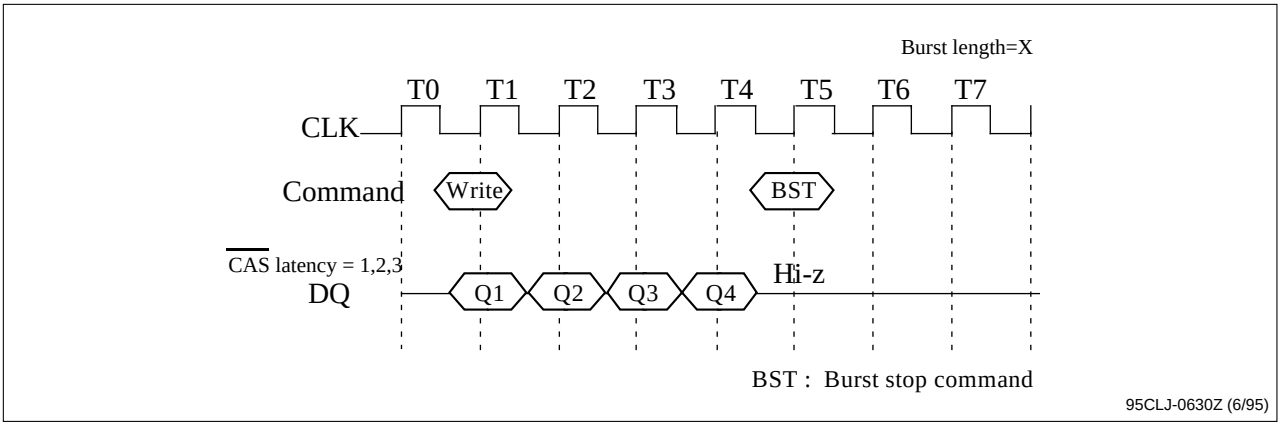


Figure 6-2. Burst Stop Command for Write



6.1.2 Precharge Command, Read Cycle

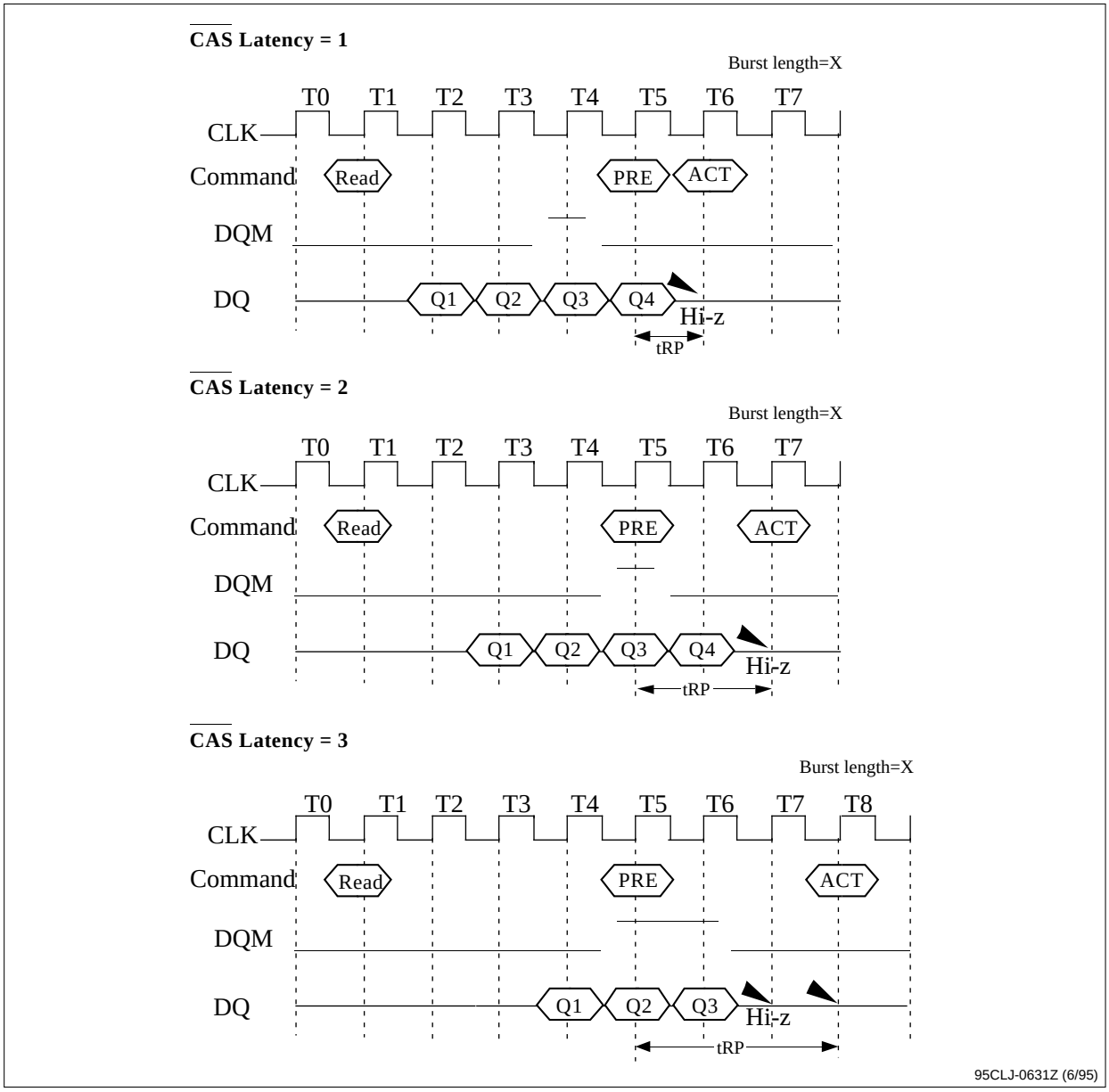
When the precharge command is asserted, the burst read operation is terminated (tRAS must be satisfied), and precharge starts. The same bank can be activated again after tRP from the precharge command. DQM must be high to mask the invalid data. See Figure 6-3.

(1) When $\overline{\text{CAS}}$ latency is 1, read data remains valid until the precharge command is asserted. Invalid data may appear one clock after valid data out.

(2) When $\overline{\text{CAS}}$ latency is 2, read data remains valid until one clock after the precharge command. Invalid data may appear one clock after valid data out.

(3) When $\overline{\text{CAS}}$ latency is 3, read data remains valid until one clock after the precharge command. Invalid data may appear one and two clocks after valid data out.

Figure 6-3. Precharge Termination for Read



6.1.3 Precharge Command, Write Cycle

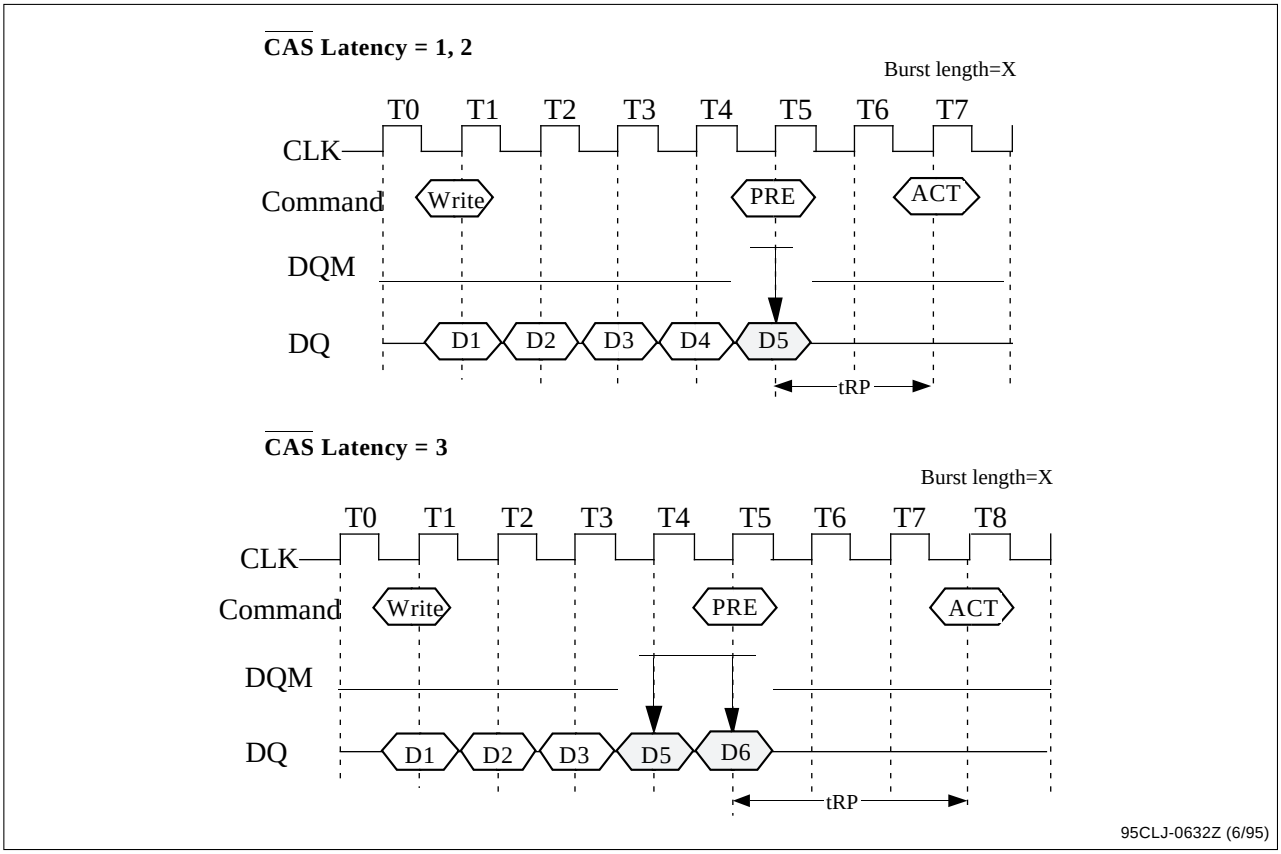
When the precharge command is asserted, the burst write operation is terminated and precharge starts. The same bank can be activated again after tRP from the precharge command. DQM must be high to mask invalid data in. See Figure 6-4.

(1) When $\overline{CAS}$ latency is 1 or 2, write data written prior to the precharge command will be stored correctly. However, invalid data may be written at the same clock

as the precharge command. To prevent this, DQM high at the same clock as the precharge command will mask the invalid data.

(2) When $\overline{\text{CAS}}$ latency is 3, write data written more than one clock prior to the precharge command will be stored correctly. However, invalid data may be written one clock before and at the same clock as the precharge command. To prevent this, DQM high from one clock prior to the precharge command until the precharge command will mask the invalid data.

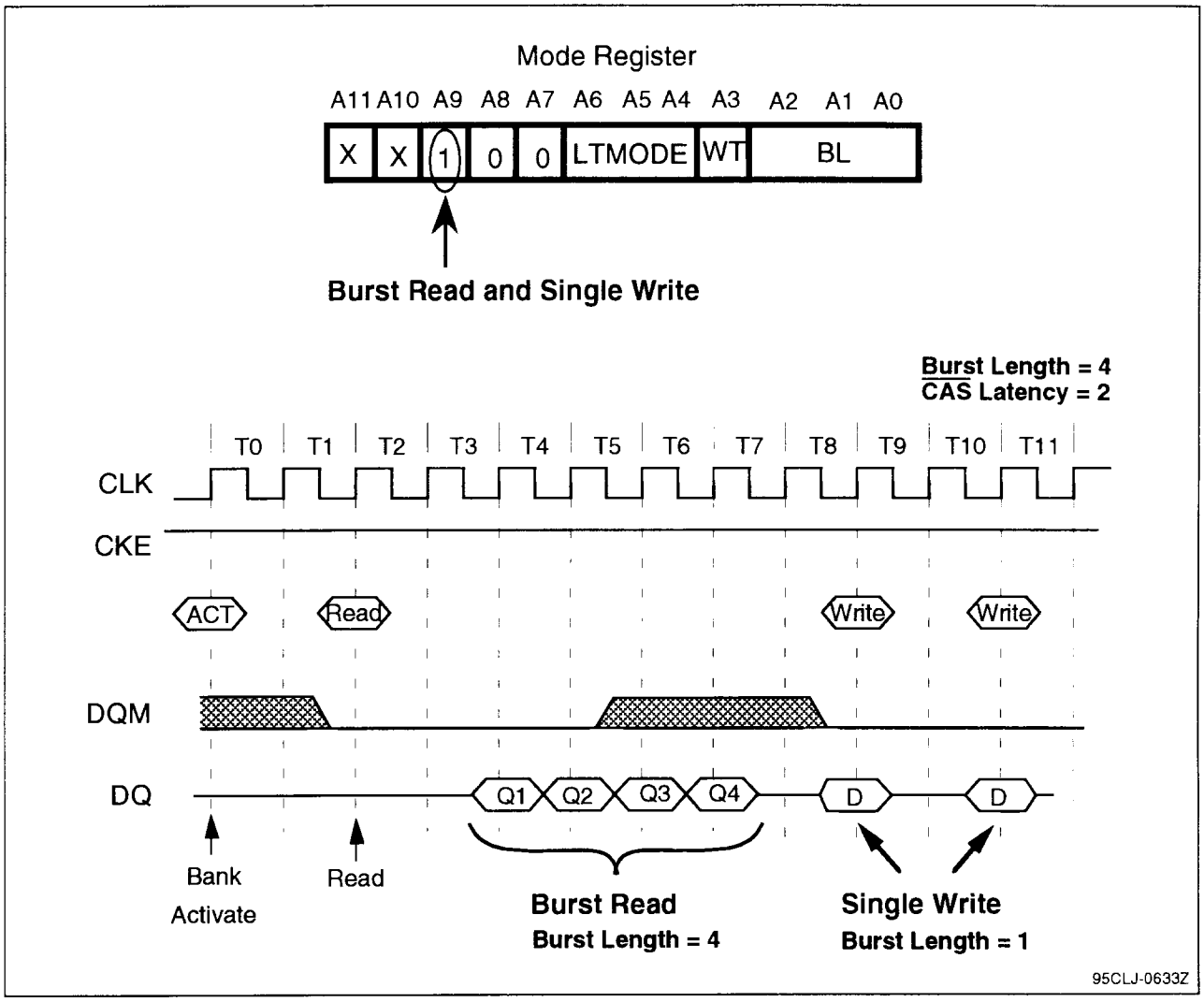
Figure 6-4. Precharge Termination for Write



6.2 Burst Read and Single-Write

The NEC SDRAM supports the Burst Read and Single-Write mode, which is suitable for some microprocessors that have a write-through cache. See Figure 6-5.

Figure 6-5. Burst Read and Single-Write



NEC

Read/Write Command 7

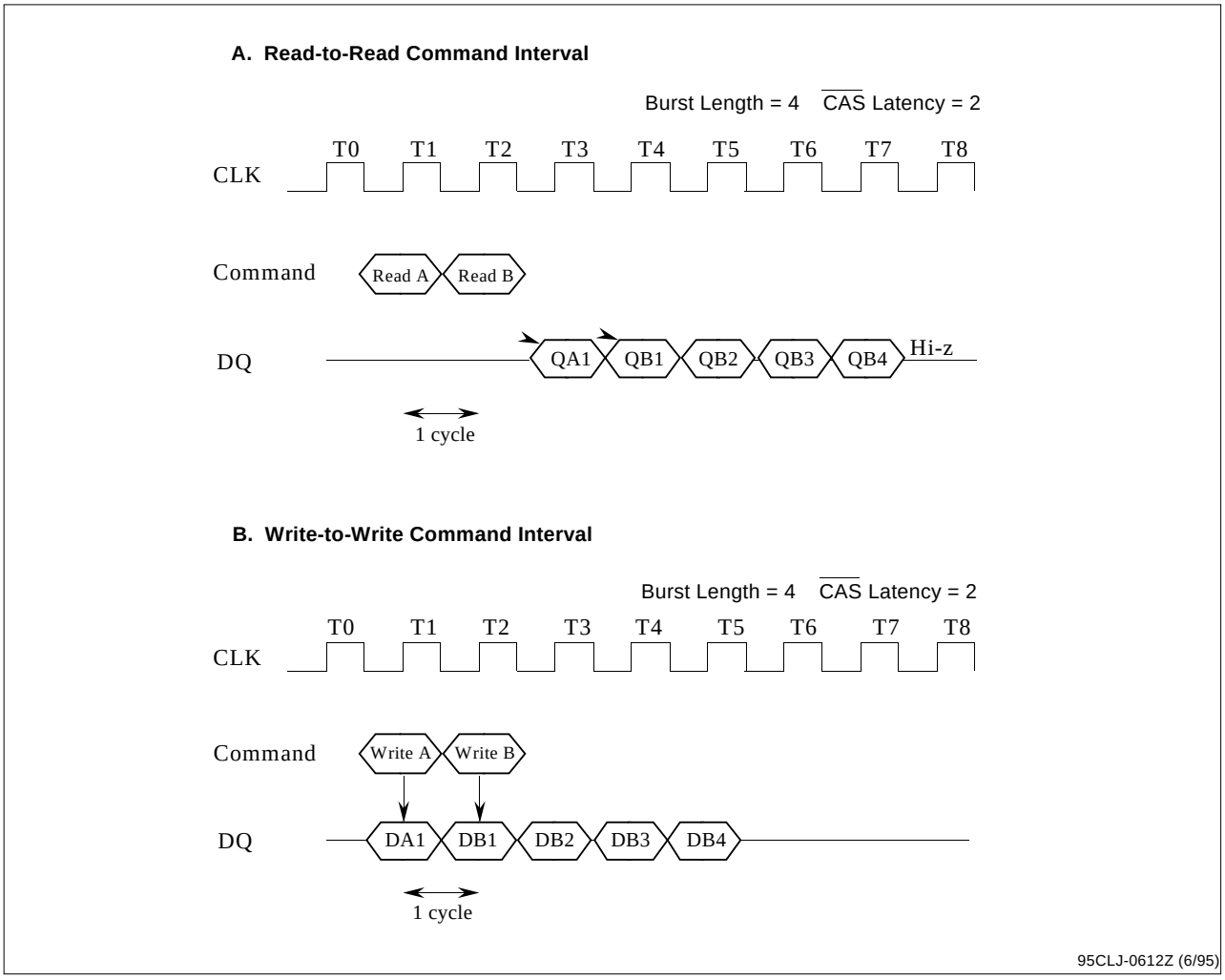
7.1 Read-to-Read Command

During a read cycle (QA1, QB1, . . .) when a new read command (Read B) is asserted, access from the second read will begin and data will be output after the $\overline{CAS}$ latency, even if the previous read operation is not completed. This means the first read will be interrupted by the second read. Read commands can be asserted at every clock without restriction. See Figure 7-1.

7.2 Write-to-Write Command

When a write cycle (DA1, DB1, . . .) is interrupted with a new write command (Write B), the previous burst will terminate and the new burst will begin with the new write command. Write A is interrupted by Write B. The minimum interval between the two write commands is 1 cycle. Write commands can be asserted at every clock without restriction. See Figure 7-1.

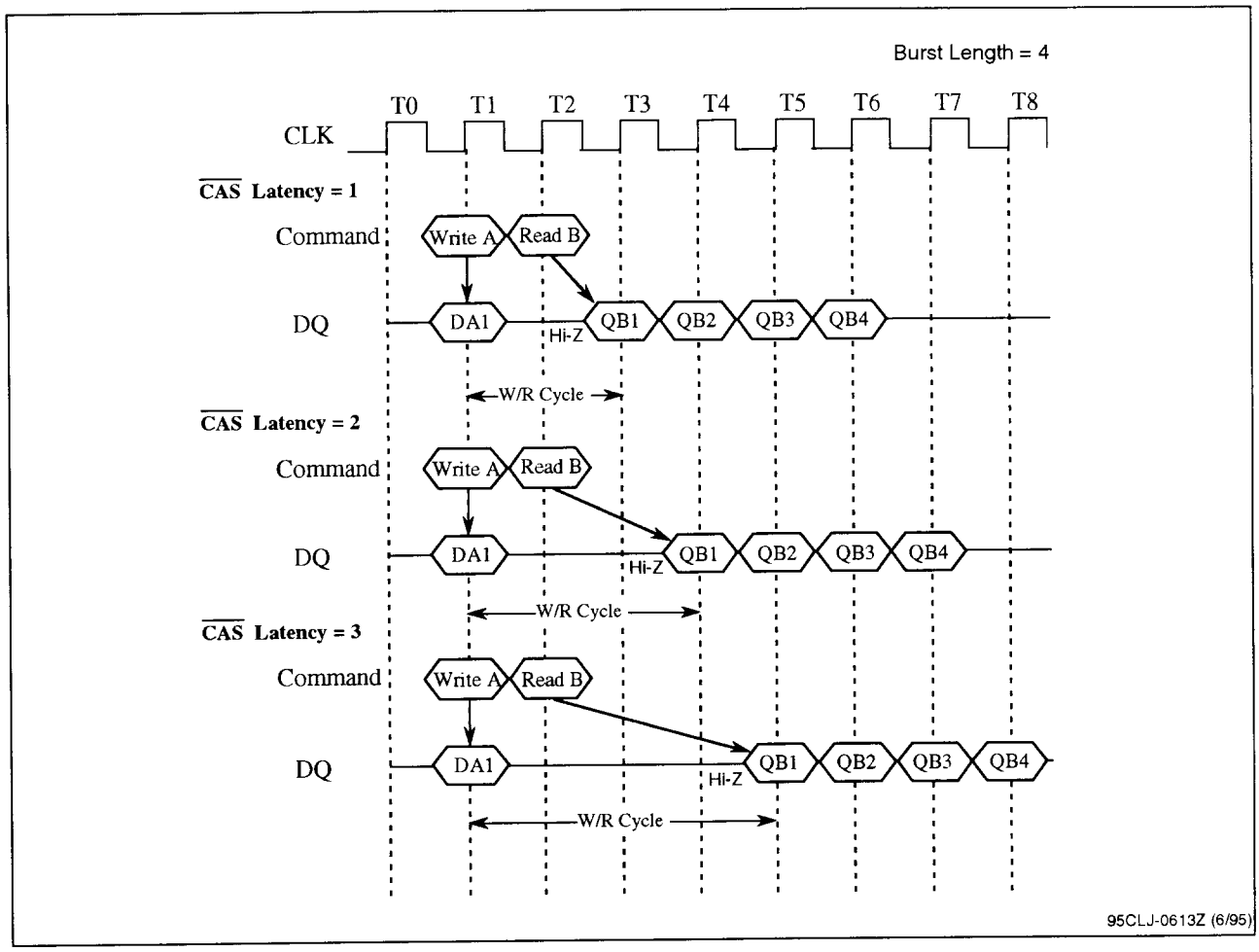
Figure 7-1. Read/Write Command Interval



7.3 Write-to-Read Command

To avoid bus contention in a write-to-read operation, it is important to ensure at least one dead cycle between write data and read data. This allows the memory controller to stop driving the data bus and the SDRAM to begin driving the bus. Any write data on the bus will be ignored as soon as the read command is issued. The write command to read command interval is 1 clock. The write/read cycle time (write-to-read operation) is equal to 1 clock plus the $\overline{CAS}$ latency. See Figure 7-2.

Figure 7-2. Write-to-Read Command Interval



7.4 Read-to-Write Command

7.4.1 DQM Function

The DQM function is equivalent to the standard $\overline{OE}$ function, which controls the output buffer and does not affect burst address generation. In addition, DQM acts as a mask for the data input buffer.

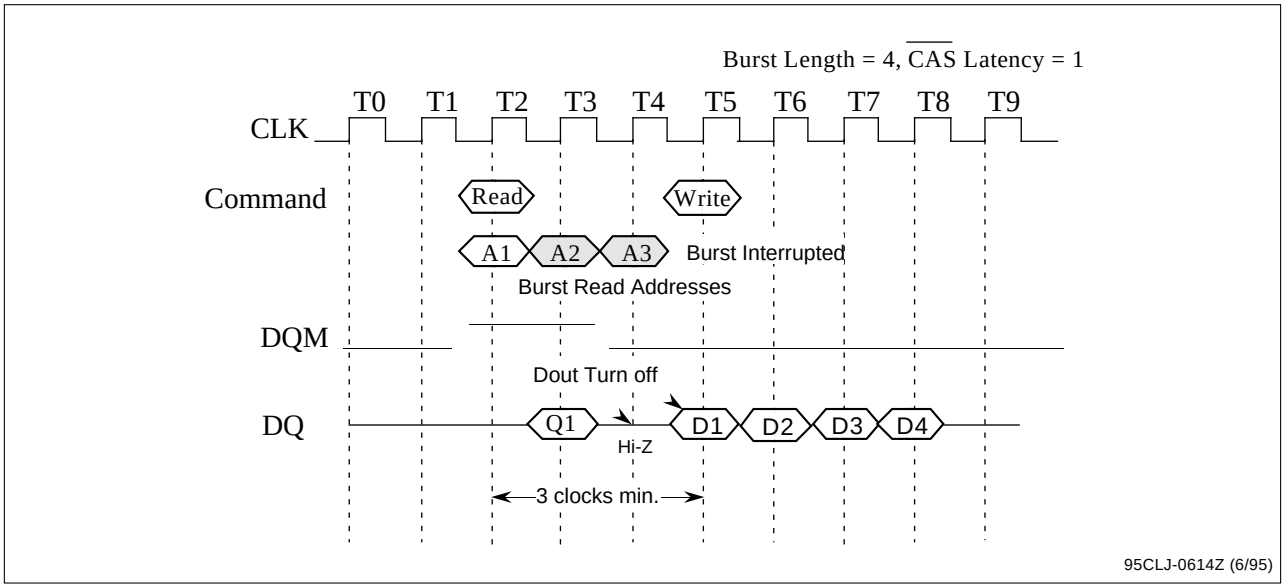
Independent of $\overline{CAS}$ latency or burst length, the DQM latency is 2 clocks for reads and 0 clocks for writes. This difference permits masking read data while allowing a write operation.

7.4.2 Read Interrupt, General Case

In all combinations of burst length and $\overline{CAS}$ latency (except 3), a read can be interrupted by a write. The minimum read-to-write interval to avoid data bus conflict is 1 cycle. The data bus must be Hi-Z, using DQM before issuing the Write command.

When a read burst begins, the internal burst read addresses are generated but generation will be interrupted by a write command. A high-level DQM must be used to turn off the output buffers to avoid bus conflict between burst read data and burst write data. In Figure 7-3 , DQM must be high at T2 to ensure the output buffer is turned off before the controller drives D1. The DQM must stay high through T3 to ensure data does not drive the bus from burst address A3.

Figure 7-3. Read Interrupt; General Case

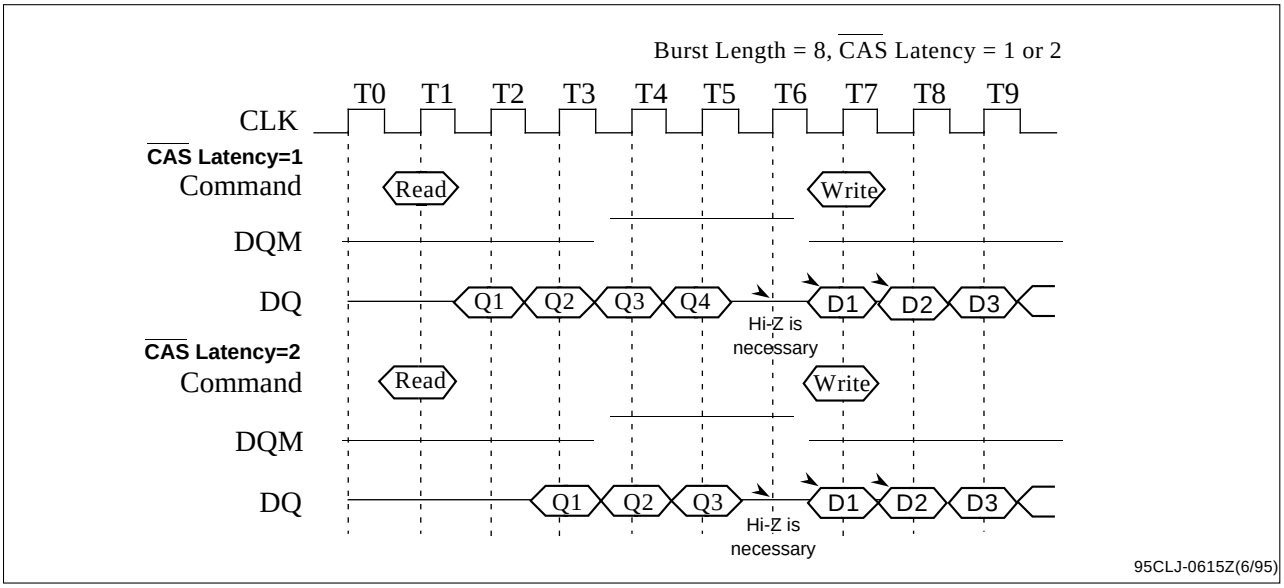


7.4.3 Read Interrupt, Special Cases

Figure 7-4 shows similar use of the DQM function in a read-to-write operation for burst length = 8 and $\overline{CAS}$ latency = 1 or 2. For $\overline{CAS}$ latency = 1, the read burst internal address is generated through T6. Data will output from the read address at T6 so DQM must remain high until T5 to turn off data at T7. DQM high at T6 is recommended because invalid data may be driven at T6

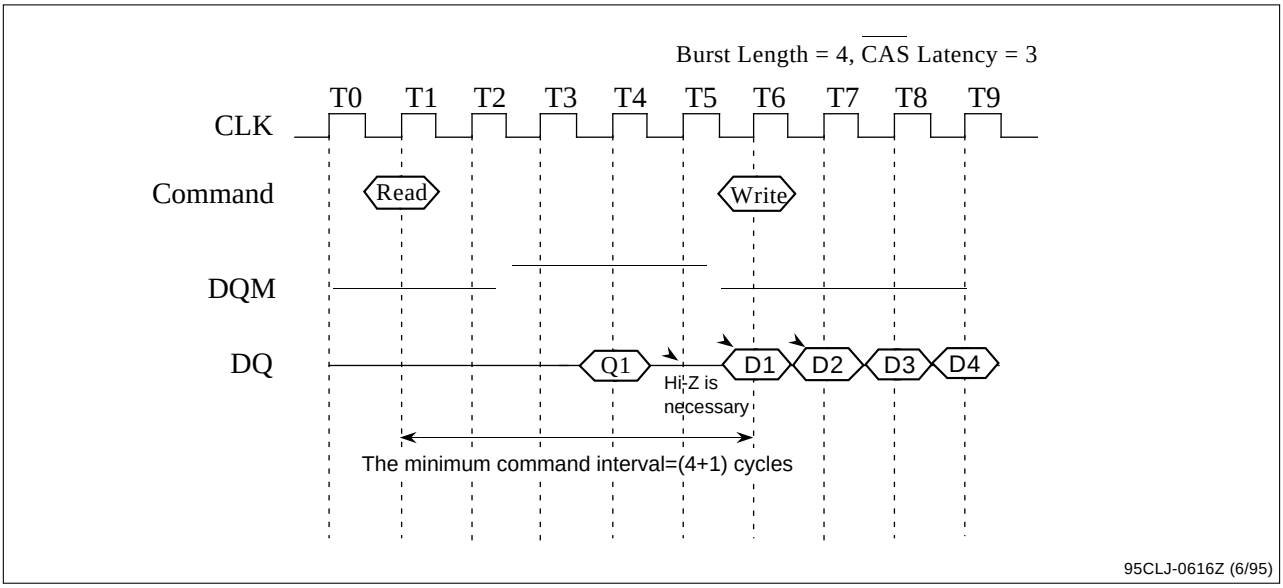
For $\overline{CAS}$ latency = 2, DQM remains high through T6 to turn off output data from the read address at T6.

Figure 7-4. Read Interrupt; Burst = 8 and CL = 1 or 2



In Figure 7-5, $\overline{CAS}$ latency = 3 and burst length = 4 (not full page); then read operation can be interrupted by a write command. The minimum command interval is burst length plus 1. DQM must be high at least 3 clocks prior to the write command. In this example, burst length = 4 so the last read address is generated at T4 and data is output from this address at T7; therefore DQM must stay high until T5.

Figure 7-5. Read Interrupt; Burst = 4 and CL = 3

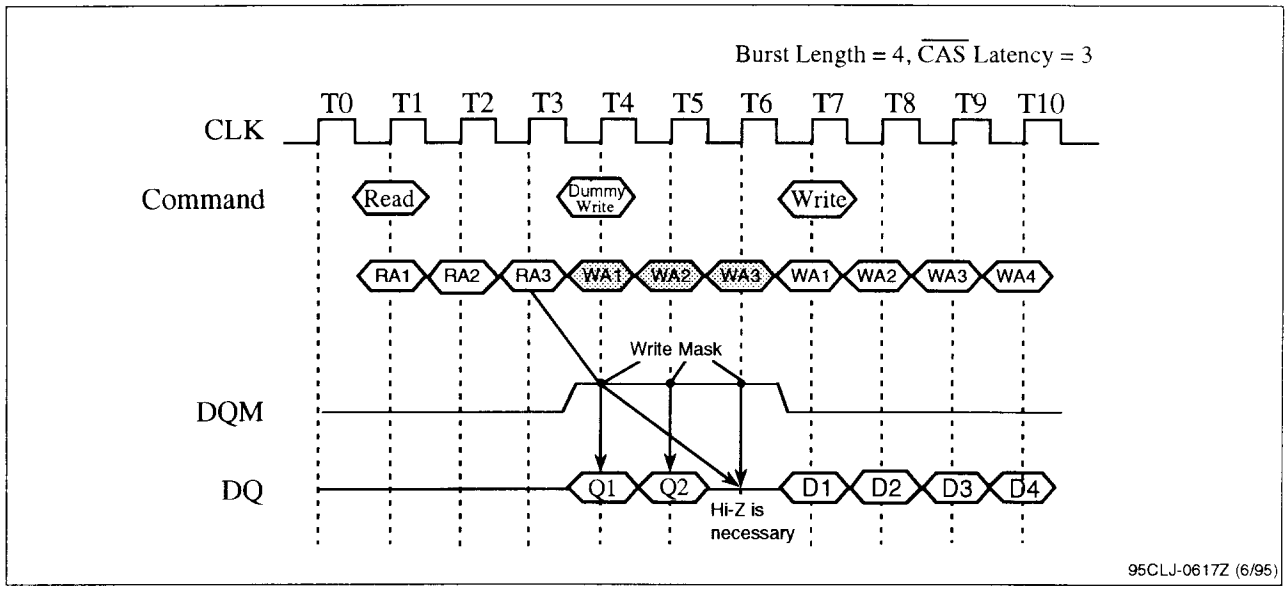


When the $\overline{CAS}$ latency = 3 for any burst length except full page, a read can be interrupted by a write but the minimum command interval between Read and Write equals the burst length plus 1. This rule has one exception: a dummy Write command

can be used to interrupt a Read; see Figure 7-6. (Write is asserted but the controller does not drive write data.) A Burst Stop command or a Precharge command is recommended for interrupting the read cycle when the $\overline{CAS}$ latency = 3.

Figure 7-6 is a good example of using a dummy write cycle to interrupt a burst read cycle. A dummy write at T4 stops the generation of read addresses. It also starts a burst write, which requires the use of DQM to mask the write at T4, T5, and T6. Also, note the use of DQM to turn off the data output generated from read address RA3 at T3.

Figure 7-6. Read Interrupt by Dummy Write



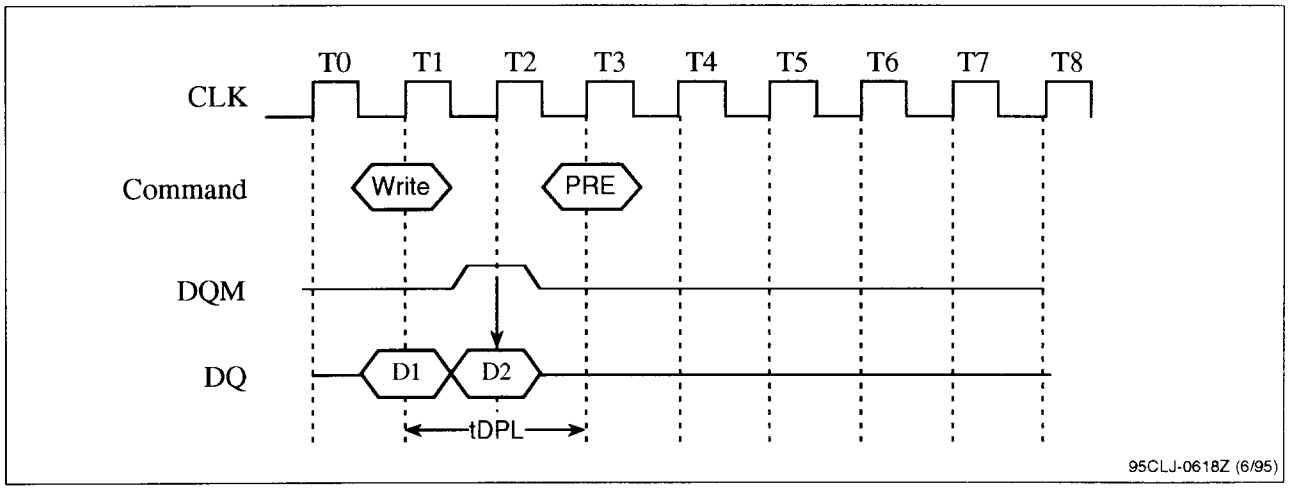
7.5 Legal Command Sequences

7.5.1 Question 1

If a Write command is issued and the DQM is used to mask the second data in the burst, when is the earliest time that a Precharge can be issued? (Clock frequency = 100 MHz)

Answer: As shown in figure 7-7, for a $\overline{CAS}$ latency = 3, the minimum time from the last data input to the precharge command is 2 clocks. This comes from the ac parameter tDPL = 15 ns minimum (-10 device), which is the earliest time that precharge can be inserted without interrupting the write cycle. Note that the tDPL minimum delay is referenced from the last unmasked data to PRE.

Figure 7-7. Precharge 1

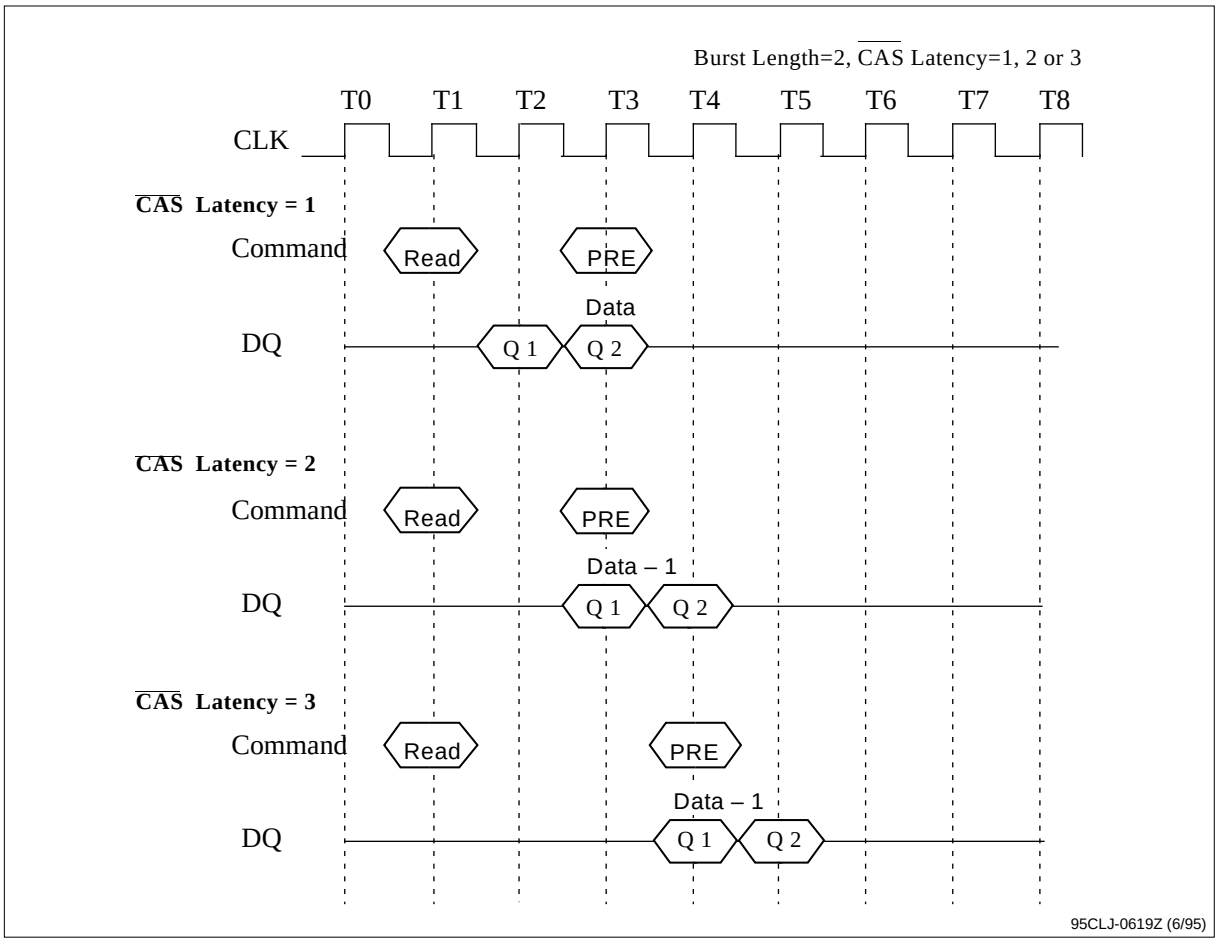


7.5.2 Question 2

What is the earliest time after a read that a precharge command can be issued without losing read data?

Answer: Depending on the $\overline{CAS}$ latency, the precharge command can be issued at the last data in the burst or at (data minus 1) in the burst. See Figure 7-8.

Figure 7-8. Precharge 2

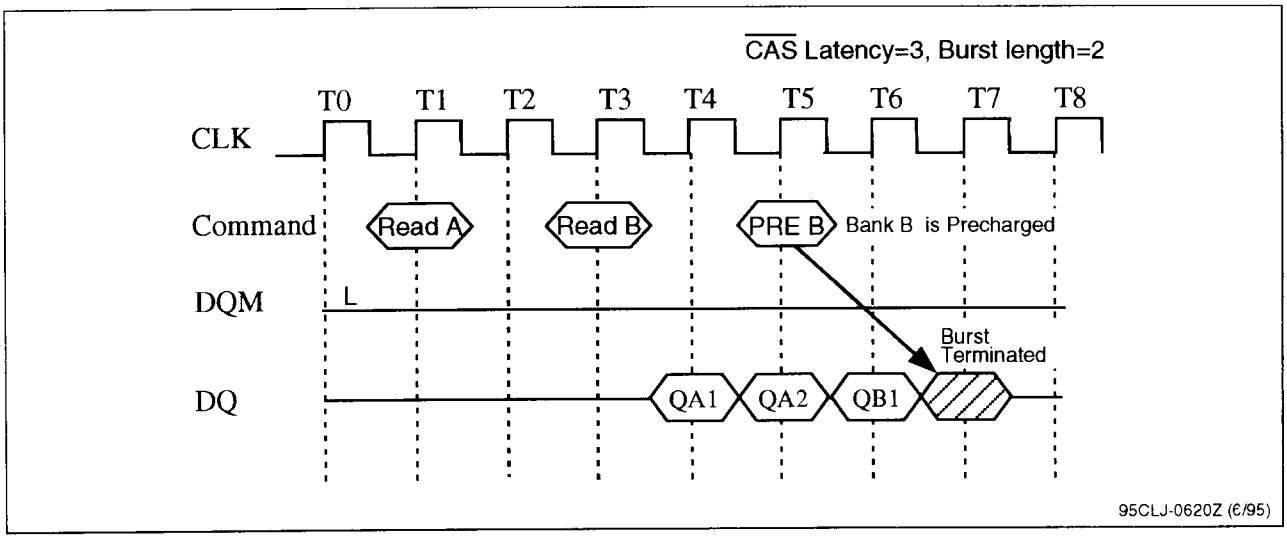


7.5.3 Question 3

In Figure 7-9, can precharge be performed at clock T5 if only QB1 is used and QB2 is ignored? That is, will issuing an early PRE command before start of the burst affect QB1 or cause any misoperations?

Answer: Even if a PRE command is issued before the first read data, the Read commmand is performed until the end of the burst or stopped by PRE command termination. The operation in Figure 7-9 is a valid command sequence.

Figure 7-9. Precharge 3



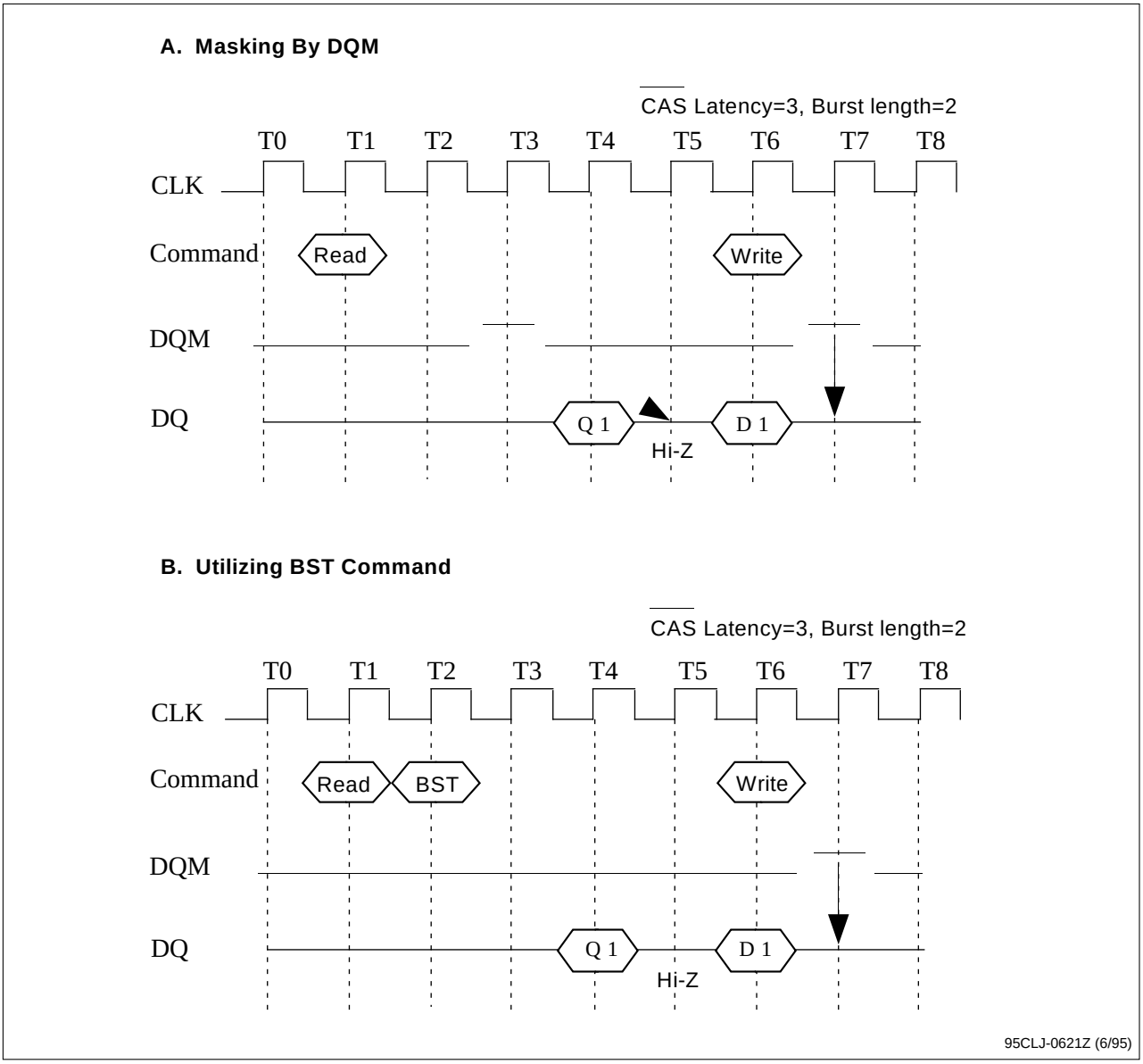
7.5.4 Question 4

What is the shortest read-to-write (read-modify-write cycle) command interval using $\overline{CAS}$ latency = 3 and burst length = 2?

Answer: Figure 7-10 shows an operation where the second data in the burst is masked by DQM to shorten the read-to-write interval to 5 clocks. Considering the operation from the CPU side, this can be used for a read-modify-write cycle where one data word is read at T1 by the CPU, modified, and rewritten (RMW) at T6.

This same RMW operation can be performed with the BST command. The BST command stops the read address generation at T2 so Q1 is output at T4 but not at T5. DQM masks the second write data D2.

Figure 7-10. Read-Modify-Write



NEC

Designing With Synchronous DRAMs 8

8.1 Clocking Requirements

The first priority of synchronous design is to establish a low jitter, noise immune, terminated transmission line for clock distribution. Poor design of the distributed clock can result in a crippled design or, more probably, one that has no chance of ever being successfully manufactured.

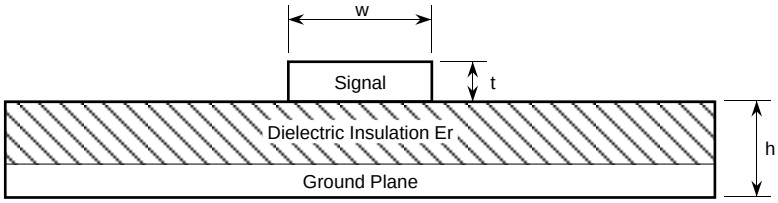
A review of transmission line physics as it applies to modern printed circuit board technology is considered important at this point.

8.2 Microstrip Physics

In Figure 8-1, equations (1) and (2) define the unloaded impedance Zo of the cross section diagrammed and the unloaded propagation time tPO of an incident wave of the cross section. Note that propagation is affected only by the dielectric constant Epsilon-r, whereas the impedance is affected by all parameters.

Equations (1) and (2) pertain to a basic, single-element microstrip transmission line and do not account for any other loading. If interconnect to several other devices is desired, solving for the loaded microstrip condition by equations (3) and (4) is required.

Figure 8-1. Microstrip Physics



Unloaded bus

(1) $Zo = 87 \times (Er + 1.41)^{-1/2} \times \ln [5.98h/(0.8\ w + t)]$ ohms

(2) $tPO = 1.017 \times (0.475\ Er + 0.67)^{1/2}$ ns/foot

For a typical bus:

t = 1.5 mils
w = 11 mils
h = 12 mils
Er = 4.7 for fiberglass
Zo = 68.33 ohms
tPO = 1.7 ns/foot

Loaded bus

(3) $ZL = Zo \times (I + CL/C)^{-1/2}$

(4) $tPL = tPO \times (1 + CL/C)^{1/2}$

For a typical bus:

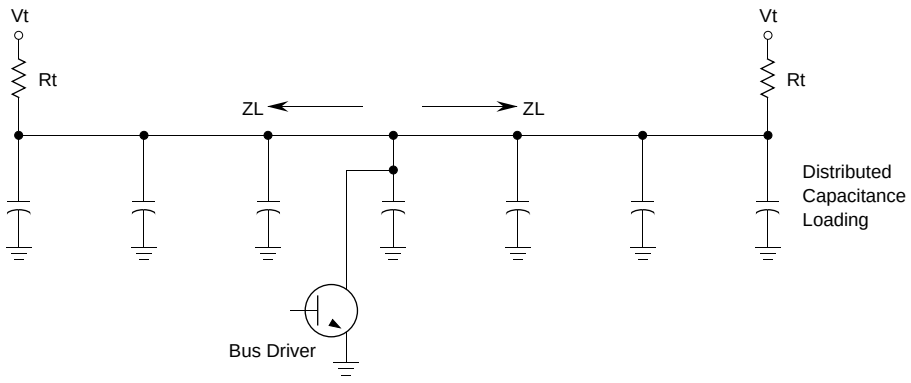
CL = 50 pF
C = 2 pF/inch x 4 inch = 8 pF
tPO = 1.7 ns/foot (144 ps/inch)
ZL = 43 ohms
tPL = 2.8 ns

95YL-0591B (6/95)

8.2.1 Driving the Loaded Transmission Line

Now let us focus on what an individual output buffer sees on the loaded transmission line. Figure 8-2 is a simplified schematic of a driver on the loaded line. Note that the driver experiences a ZL in two directions on the line, whether the line is terminated or not. This results in the driver seeing one-half the line's loaded impedance, or ZL/2.

Figure 8-2. Driving the Loaded Transmission Line



95YL-0592B (5/95)

To drive the bus properly requires a driver capable of the following:

ID = (Voh - Vol) / ZL / 2

or in the case of an LVTTL driver:

ID = 1.6 V / 27 ohms / 2 = 30 mA (50-pF loading)

The 1.6-volt switching delta is the minimum slew to satisfy the LVTTL output voltage high and low levels (Voh and Vol). This is a fair amount of drive for DRAM LVTTL I/Os, which generally have a maximum I/O drive of ±8 mA. Realize that a doubling of the rise time will be observed to propagate a wave down both ends of the transmission line at this drive level.

It is important to note that between the 10% and 80% switching levels, dV/dt is essentially linear and dependent on the ZL/2 of the transmission line. This can be viewed as a rise time vector (or fall time vector, given the same pulldown capability) that is rotated ever more toward the horizontal as the capacitive loading increases. The net result is decreased transmission line performance.

8.2.2 Ringing

Control of transmission line ringing is mandatory in the design of high-performance memory systems. Figure 8-3 shows the near-ideal response of the transmission line to the output excursion of an ideal driver compared to the SDRAM driver.

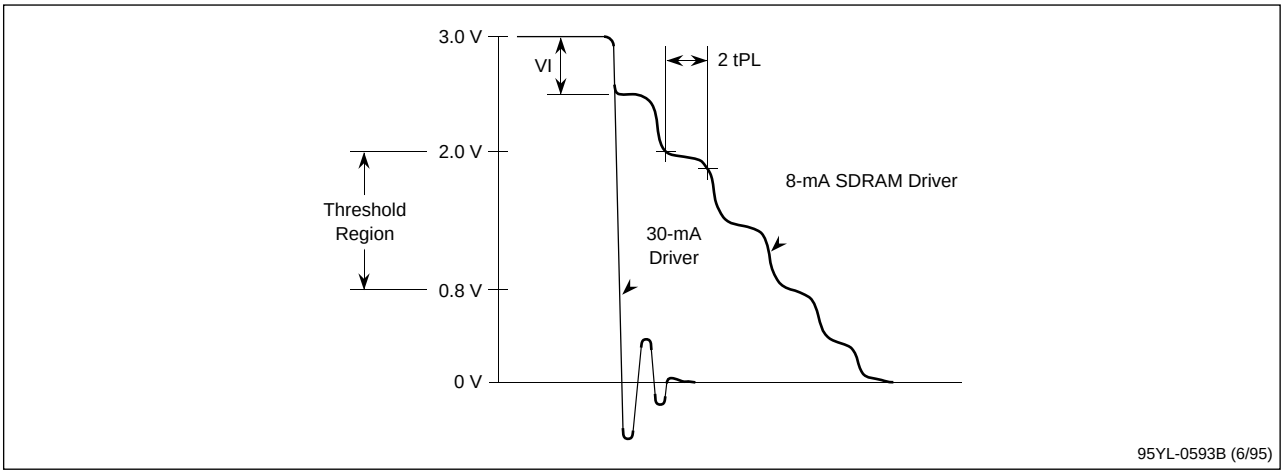
The wave in the ideal case drops through the threshold region to ground with minimal ringing in the ground region due mainly to the non-ideally terminated stubs of the interconnected devices. Conversely, the wave created by the SDRAM output driver flows down the line past distributed inductive, capacitive, and resistive obstacles, finally encountering a termination resistance. In the ideal case, the termination properly absorbs the transmitted energy of the original wave, but in this case a portion of the wave is reflected due to mismatch between the originating drive capability and reflections produced by the multiple reflective non-ideal stubs.

These interconnecting stubs add a complex component to the real and imaginary components of the transmission line that vary depending upon their number and the point of measurement.

Figure 8-3 also shows the reflected component from the terminating (or nonterminating) components. Note that the loaded propagation time is of key interest here as the “flight time,” equal to twice the tPL (down and back) to the point of origination. The reflected wave becomes opposite in polarity after reflecting off the termination. Thus its component subtracts instantaneously from the voltage level at the driver, resulting in a flattening of the signal or even an apparent reversal in signal direction.

This can be viewed as the original wave reflecting back and forth along the transmission line, diminishing in amplitude with each end termination encounter. (This is not to mention the sub-reflections from the multiple stub devices that are not ideally terminated but nevertheless must be interconnected). The cumulative term for this is “ringing.”

Figure 8-3. Transmission Line Ringing



8.2.3 Summary

The transmission line interconnecting the clock generator, memory controller, and memory array is of overriding importance in the success of any high-performance system design. The physical printed circuit board can to a certain extent control the unloaded and loaded characteristics, but after a certain range cannot provide any further practical improvements because trace width becomes much too narrow and distributed resistive elements become controlling factors. The number of stub elements can be controlled by limiting the number of interconnects. The end solution will differ greatly depending upon the application and the tradeoffs made. These are the domain of the designer’s decision-making process.

8.3 Clock Stability

Clock stability is a major concern in the design of high-perfomance memory systems. As system clock frequency trends upward, designers must take into account the stability of the clock subsystem. An expression of the variation encountered in a clock network is:

Tolerance = Intrinsic skew + Extrinsic skew + Jitter

(1) Intrinsic skew is the variation found in the clock buffer. It is usually specified as pin-to-pin skew for a group of clock buffers. We will assume the use of a single-chip solution.

(2) Extrinsic skew is the delay variation attributed to effects in the interconnect.

(3) Jitter is the clock-to-clock variation in the arrival time of the clock. Its effect stems mostly from noise in the power environment causing time varying shifts in the input threshold of the receiving device.

Extrinsic skew can be futher broken into three major components:

Extrinsic skew = TOFdelta + Distd_delta + MT

(1) TOF delta is the variation in flight time of the undistorted signal because of unequal line lengths. It is best controlled by equalizing all net lengths to that of the longest clock.

(2) Distd_delta is the distortion-delay variation. The propagated signal undergoes a lowpass filtering effect due to the distributed capacitive load of the transmission line. The net effect is to lower the rise time, resulting in an additional delay in reaching the threshold value.

(3) MT is the manufacturing tolerance of the delay. It ranges from 2 to 7 ps/inch delay.

Therefore overall clock tolerance can be written as:

Tolerance = Int skew + TOFdelta + Distd_delta + MT + Jitter

8.3.1 Clock Generator

The clock internal skew resides with the clock generator manufacturer. The other parameters are due in effect to the physical design of the clocking net. To minimize these parameters, the following feature set is recommended in the selection and/or design of the clock generator:

(1) Phase-locked loop with reference crystal-controlled input and feedback clock to cancel device transit or propagation delay time (zero buffer delay).

(2) Separate analog PLL and Vdd supplies with generous decoupling capacitors.

(3) 3.3-volt ±10% Vdd compatible operation.

(4) Low-temperature coefficient crystal (≤100-200 ppm/˚C).

(5) When multiple clocks are required, individual driver output skews must be < 500 ps.

(6) Output drivers must be capable of driving four loads on a moderate length (≤ 5 inches) terminated transmission line at moderate frequencies (≤ 75 MHz) and two loads at high frequencies (75 to 100 MHz).

(7) Output buffer designs capable of “doubling up” to drive heavily loaded lines, if necessary.

8.3.2 Clock Generator Layout

The following requirements are recommended in design of the memory system clock generator:

(1) Clock traces must be of equal length and impedance.

(2) Treat clock traces as transmission lines with controlled impedance. Minimize clock trace length and loading.

(3) Determine clock signal termination type early in the design. Series termination will reduce the termination power requirement, but the loads must be clustered at the end of the clock lines, implying stubs shorter than 2 inches.

(4) Clock signal loads must be equal (1 pF difference implies a 50-ps delay).

(5) Clocks distributed across backplanes should be point-to-point. This removes the “flight time” skew introduced as the signal propagates down the backplane past each board (i.e. memory modules).

(6) Microstrip is preferred over stripline because propagation is faster (150 versus 200 ps).

(7) Use transmission lines with an impedance as high as possible for improved noise immunity. Recommended:

Microstrip; dielectric = 4.7 @ 0.012” thick
Conductor; 0.011” wide x 0.0015” thick copper

(8) In module-based systems, include connector and PCB model in simulations.

(9) Avoid through-hole interconnects; they add 2 or 3 pF to the transmission line.

(10) Always be generous with decoupling capacitors.

These recommendations are considered the minimum necessary to begin modeling the intended design’s transmission line performance through simulation on a Spice model. NEC makes available the Synchronous DRAM HSpice model on a non-disclosure agreement basis.

8.4 Design Considerations

Input/output loading (DQs) is an important parameter of any memory design. In a lightly loaded system (≤30 pF), designs can use less than optimum techniques to achieve reliable clocking (such as source series and asymmetric termination). Light

loading is also synonymous with fewer devices, having the effect of shorter interconnect traces with the devices physically located nearer to the controller and in most cases soldered directly to the motherboard.

In a moderately loaded system (≤50 pF), designs must begin using minimum transmission line requirements. Line length, balance, termination, output drive matching, and number of stub loads become overriding in their importance.

At this point, whether the design will include memory modules must be decided. Memory modules add capacitive, inductive, and propagative factors that need to be considered. The inclusion of multiple memory devices with their own complex loads further complicate the design equation.

The decision to buffer must be made at this threshold. Buffering decreases the loading on the clock generator and memory controller so that the system can operate through a range of module configurations from a minimum to a maximum number.

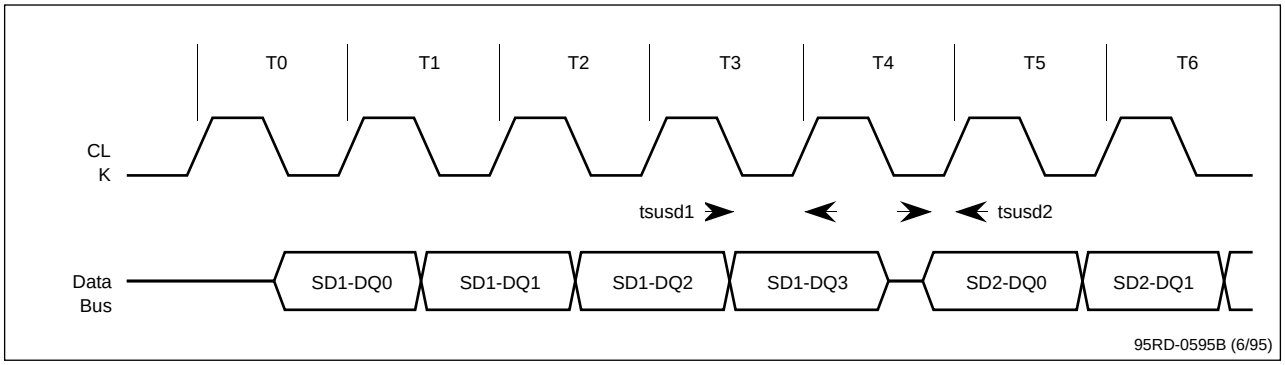
The best solution for this problem is the divide-and-conquer algorithm. The use of signal buffering is well known. With the availability of phase-locked loop, zero-delay buffers, it is possible to redrive the clock without adding much additional delay. A rule of thumb for the current generation of synchronous DRAM memories is that registered buffering is mandatory above 50 MHz or in heavily loaded systems (50 to 100+ pF).

In the following examples, assume the clock is PLL buffered and the control inputs are registered.

8.4.1 Registered/Buffered Design

First, a model must be developed to ascertain critical path parameters necessary to understand the worst-case design scenario. It is important to develop a system viewpoint of the critical time window in which data will be made available on the memory data bus to the controller. The data setup and hold time specifications become very critical in this case. Figure 8-4 shows timing for the case where the synchronous DRAM is outputting data on the data bus (read case).

Figure 8-4. Read With Gapless Data I/O



The difference in flight time between SDRAM1 and SDRAM2 to the memory controller is the difference in time Tdelta. Futher, the overall clock skew (Tskew) and the memory controller setup (Tsetup) times must be added to the equation. Thus, the following equation is used to derive the the true system timing required to satisfy the available data window for the controller:

$$Twindow_{min} = Tcycle_{min} - Tacc_{max} + Thold_{min} - (Tskew_{max} + Tsetup_{max} + Tdelta_{max})$$

The specifications of the NEC 100-MHz SDRAM show a Tacc of 9 ns and a Thold of 4 ns so that the sum of (Tskew + Tsetup + Tdelta) equals 5 ns. Using 1 ns for Tskew and 2 ns for Tsetup yields a Tdelta of 2 ns for a Tcycle time of 10 ns, which is about 3 inches between SDRAM1 and SDRAM2. The calculation does not take into account any further delays on the memory module.

Assuming that these delays add an additional 250 ps to the equation allows a system design that is constrained to less than 3 inches in transmission line length and capable of operating at 80 MHz using 100-MHz rated synchronous DRAMs. It also assumes a phase-delayed read clock to the controller from the clock generator.

The following equations calculate the minimum difference in propagation between the DQs of the two devices:

$$Tpd' = Tpd\ (1+ CL/(LCo)^{1/2}$$

Tpd Propagation rate of the unloaded transmission line.
CL Load capacitance (distributed)
L Line length
Co Unloaded capacitance of the line

The delay of flight time and distortion delay can be calculated from:

$$LTpd' = LTpd\ [(1 + CL_{max}/LCo)^{1/2} - (1 + CL_{min}/LCo)^{1/2}]$$

Knowing the minimum and maximum values of CL, we can now compute the minimum and maximum delays for a given lossless transmission line. For a load of four devices spaced 0.5 inch apart, the maximum delta between module 1 and module 4 is:

LTpd'/ inch = 383 ps/inch - 272 ps/inch = 111 ps/inch
(17 pF unloaded versus 40 pF loaded)

Flight time for the four-load case = 2.5 x 383 = 958 ps

Flight time for the single-load case = 2.5 x 272 = 680 ps

This indicates that an incident wave will reach threshold value 278 ps earlier in the unloaded case than in the loaded case. The four-load case of 958 ps will need an additional 250 ps of flight time when on-module I/O, trace, and connector loadings are taken into account (958 + 250 = 1208 ps).

This minimum of 1208 ps for the worst-case propagation delay is rounded up to 1500 ps, yielding a 500-ps margin in our original equation. Tdelta in this case is now improved by 500 ps, increasing the Twindow time to 5.0 ns for the 80-MHz system.

8.4.2 Buffering Requirements

Figure 8-5 is the block diagram of the JEDEC standard for the 200-pin DIMM (Dual Inline Memory Module), 2M x 8 SDRAM. The buffered or registered signals include:

Row address enable	$\overline{RE}$
Column address enable	$\overline{CE}$
Address inputs	A0 - A15
DQ mask	DQMB0 - DQMB7
Clock enable	CKE
Chip select	$\overline{CS0}$

Registering these signals implies that a clock cycle is required to allow for the registers' inherent propagation delay; it must be considered in the controller design.

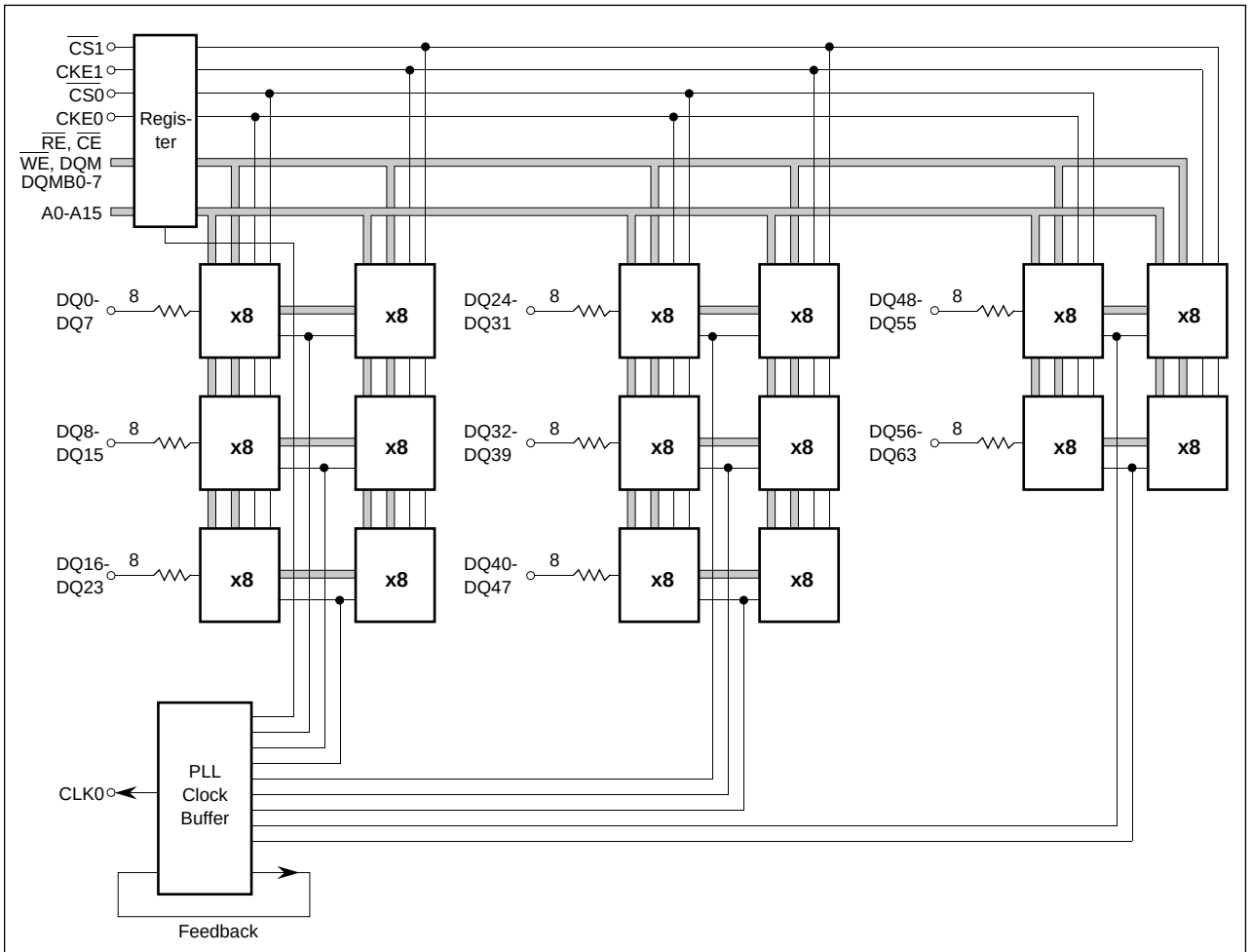
The clock input is PLL buffered and distributed to two SDRAM devices to ensure low loading on the clock signals. A rule of thumb is that the on-motherboard clock buffer has 500 ps maximum skew, and the on-module buffer adds another 500 ps for a system total of 1 ns. All clock line outputs from the PLL buffer shall be equal length to minimize on-module flight time.

Notice that a 10-ohm series resistor is specified for each DQ. The resistor is external to the SDRAM device. It can be integrated into the printed circuit board using planar resistor technology (PRT) in which the resistors are buried or embedded in the PCB.

The resistance accuracy is 5%, even though the standard requires only 20%. Use of these resistive elements is based on extensive simulations that showed a small source series terminating resistor markedly improved transmission line characteristics.

In fact, the resistor raises the transmission line impedance for a closer match with the driver output impedance. The terminating resistor also acts to roll-off the dynamic response of the driver, limiting the high-frequency spectral content that would otherwise reflect off the nearest stubs, resulting in a less than optimum transmission line envelope.

Figure 8-5. Eight-Byte DIMM Block Diagram



Notes:
1. A 10-ohm ± 20% resistor shall be wired in series with DQ0...DQ63 near the card edge connector.
2. All clock line outputs from the PLL Clock Buffer shall be equal length.

95YL-0590B (6/95)

8.4.3 Layout Recommendations

The physical locations of the major signal groups on the JEDEC Standard DIMM (Figure 8-6) are instructive as the placement strategy was at all times to limit line lengths and hence signal flight time. This is especially true for the DQ pins, which out of necessity require short lead lengths.

Two pins have been reserved for an input comparator referrence voltage (Vref). This will enable a new high-performance, low-voltage-swing interface to be used in the future.

There is new nomenclature for power supply pins: Vdd and Vddq. EIA/JEDEC now recognizes the interface to be separate from the chip array supply resulting in chip supplies being termed Vdd and interface supplies Vddq. Also, Vcc by EIA/JEDEC definition is +5 volts whereas Vdd represents all other voltage levels. The current generation of NEC SDRAMs use 3.3 volts ±10%. Note that there are 9 Vdd and 20 Vddq pins. The arrays are separate from the interface supplies and use fewer pins because their power requirements are much less than high-performance interface drivers. The power pins are distributed accordingly for minimum ohmic values between motherboard and module. Power and ground planes are highly recommended if not mandatory.

The physical placement of the SDRAMs has to be as close to the module connector as possible without violating the no-place JEDEC JC-11 standard drawings. It is recommended that the devices be placed pin 1 down or closest to the module connector to facilitate the shortest DQ lead length. The control signals being buffered have adequate setup and hold times so their placement is not as critical.

Figure 8-6. Eight-Byte DIMM Pin Configuration (Sheet 1 of 3)

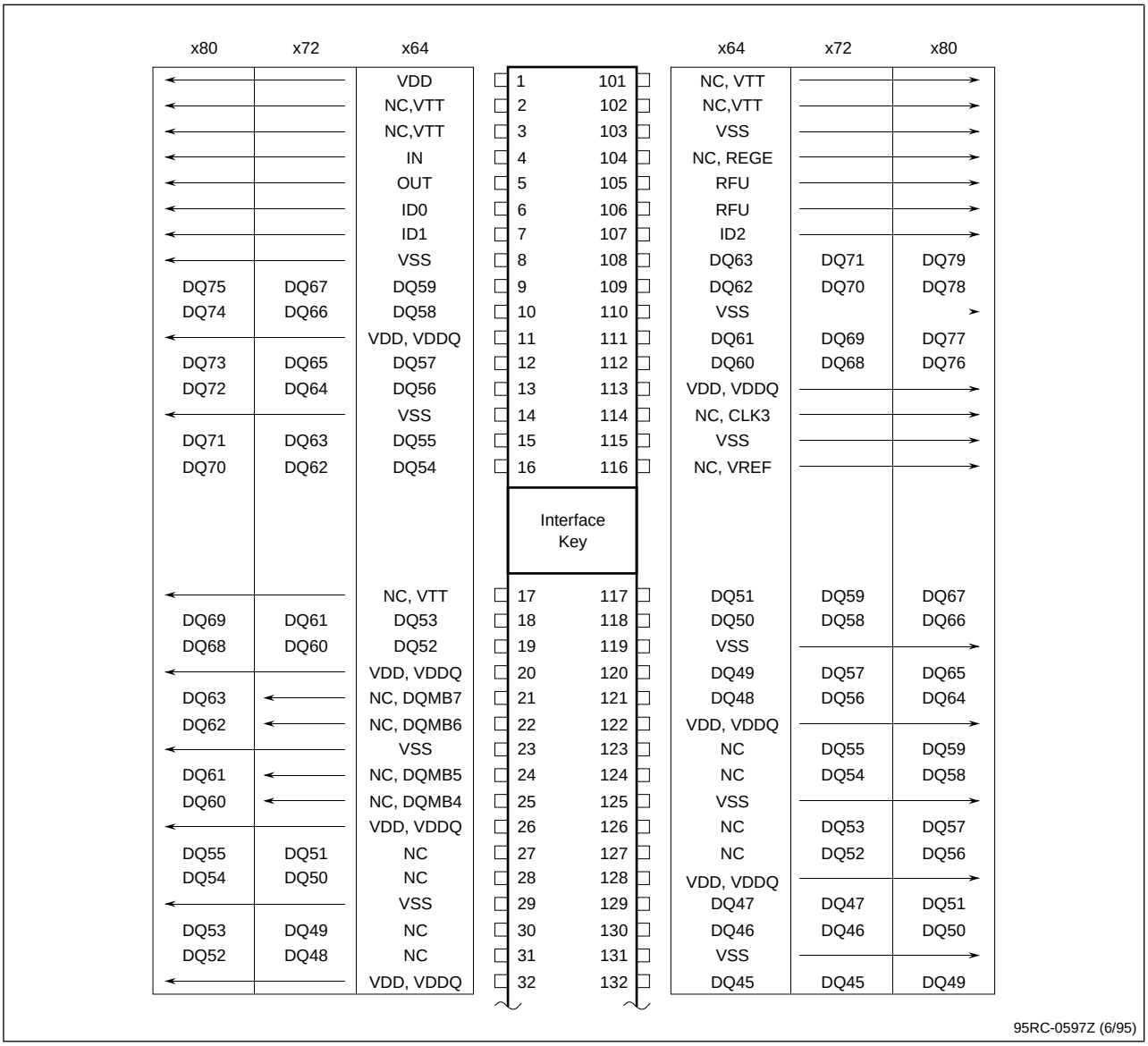


Figure 8-6. Eight-Byte DIMM Pin Configuration (Sheet 2 of 3)

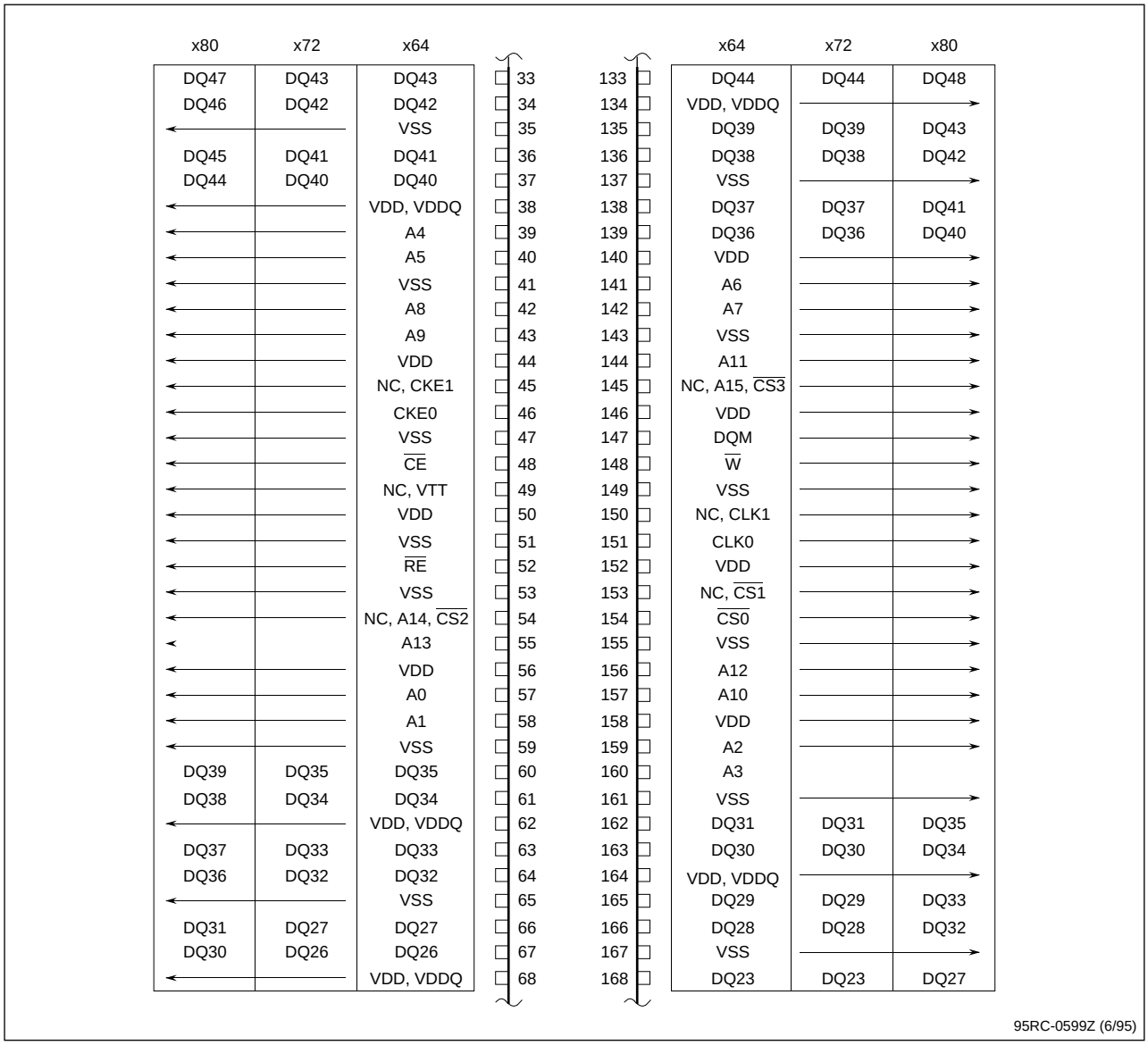
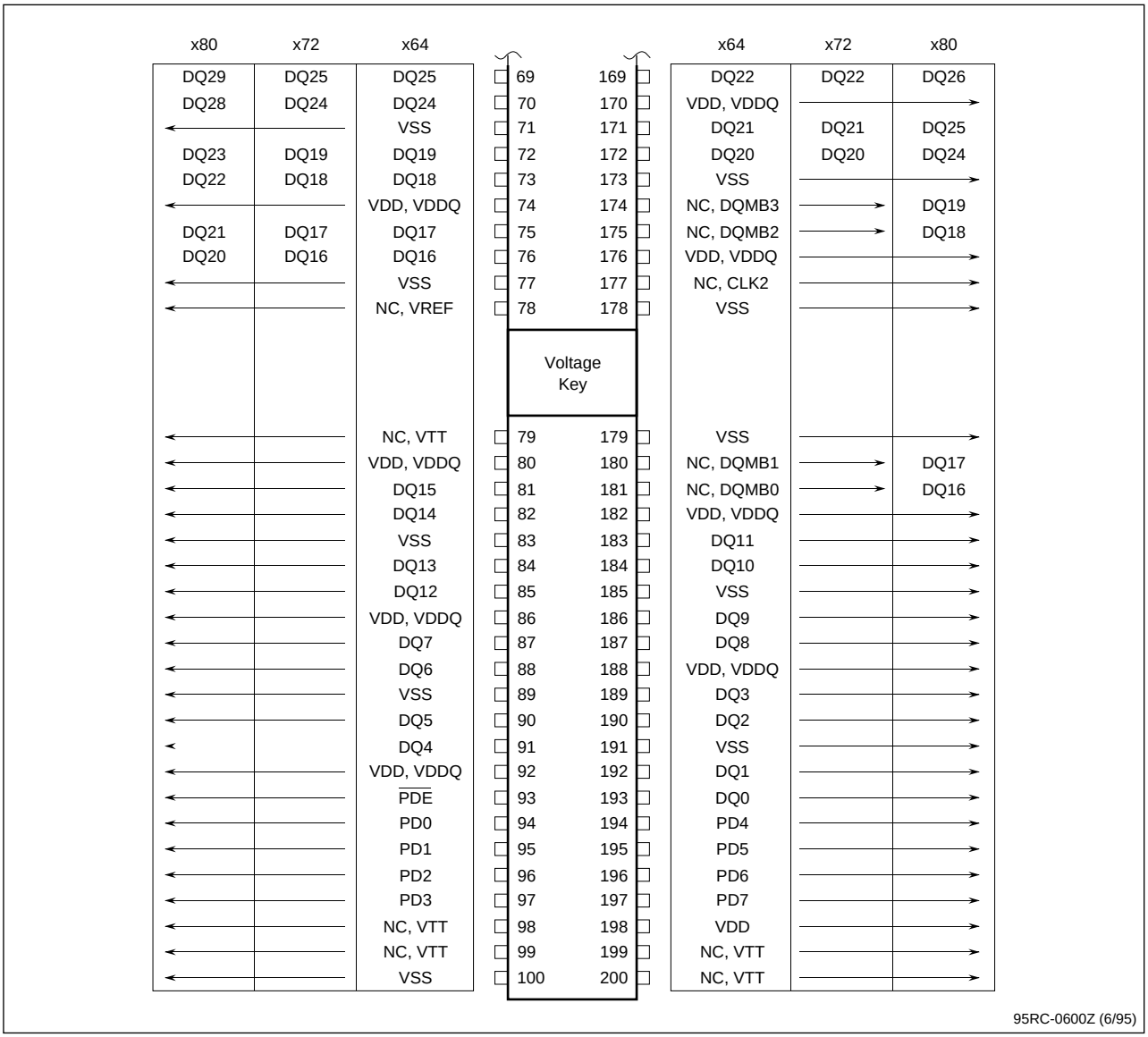


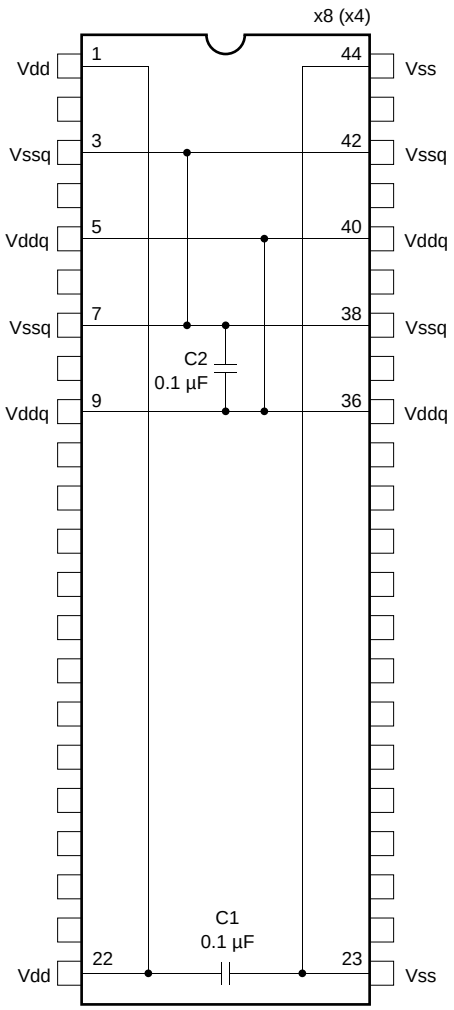
Figure 8-6. Eight-Byte DIMM Pin Configuration (Sheet 3 of 3)



8.4.4 Decoupling

Figure 8-7 shows the recommended capacitive decoupling for the x4 and x8 SDRAMs. Two 0.1-µF surface-mount capacitors are recommended each for decoupling Vdd and Vddq. A problem might be encountered here when the device is mounted with pin 1 nearest the DIMM connector pins as previously recommended. Capacitor C2 in this case would add several millimeters to the DQ trace lengths due to its mounting midpoint between pins 1 and 44. The TSOP (II) package has no clearance under the device for surface-mount capacitors as the SOJ package has.

Figure 8-7. Capacitive Decoupling for Vdd and Vddq



95RD-0596B (6/95)

8.5 Power Calculation

The power requirements of the SDRAM depend on the operational mode programmed in the power-on-reset sequence and the type of access being performed. The following currents are average currents and are classified by the different cyclic events involved in data access. The two major categories involve system and specification parameters. System parameters are application generic whereas specification parameters are from the individual device data sheet. One rule of thumb is that the higher the performance and the higher the number of DQs per device, the higher the supply power.

Current calculation formulas are in Figure 8-8. Typical average current values are shown in Figure 8-9.

Figure 8-8. Single- and Dual-Bank Current Calculations

A. Single-Bank

$$I\,(mA) = \Big[Icc2N \times \{tRP - (AN + RN) \times tRPmin\} \times tCKmin / tCK + Icc1 \times AN \times (tRASmin + tRPmin) + Icc4 \times (BN - AN) \times tCKmin + Icc5 \times RN \times (tRASmin + tRPmin) + Icc3N \times \{tRAS - (AN + RN) \times tRASmin - (BN - AN) \times tCKmin\} \times tCKmin / tCK \Big] \div T$$

B. Dual-Bank

$$I\,(mA) = \Big[Icc1 \times CN \times (tRASmin + tRPmin) + Icc4 \times (DN - CN) \times tCKmin + Icc5 \times RN \times (tRASmin + tRPmin) + Icc3N \times \{tRAS - RN \times tRASmin - DN \times tCKmin\} \times tCKmin / tCK \Big] \div T$$

Parameters

tCK	Clock cycle (ns)
tRAS	RAS active time (ns)
tRP	RAS precharge time (ns)
Precharge standby current	Icc2N (mA)
Active standby current	Icc3N (mA)
Operating current	Icc1 (mA)
Burst mode current	Icc4 (mA)
Refresh current	Icc5 (mA)
Self-refresh current	Icc6 (mA)

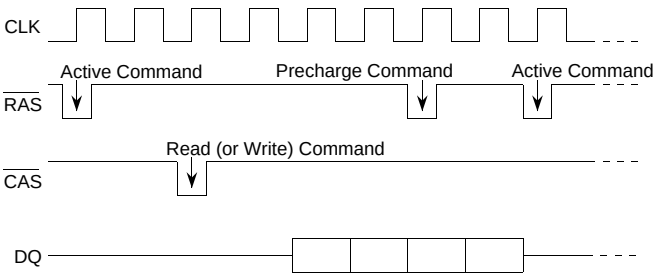
AN	Number of single-bank row activate commands
BN	Number of single-bank burst data transfers
CN	Number of dual-bank row activate commands
DN	Number of dual-bank burst data transfers
RN	Number of refresh commands
T	Combined toal elapsed time of operation
I	Average calculated current (mA)
S	Self-refresh period (ns)

95RC-0598Z (6/95)

Figure 8-9. Typical Average Current Values

A. Single-Bank, CAS Latency 2, Burst Length 4, Organization x8

- tCK3 = 10 ns
- Constant access with 2K/32 ms Auto-Refresh
- CKE high; $\overline{CS}$ low

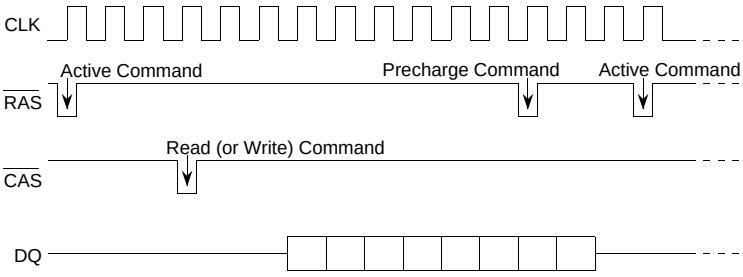


System Parameters

tCK	15 ns
tRAS	256K x 90 ns + 2K x 70 ns = 24.0 ms
tRP	32.0 ms – 24.0 ms = 8.0 ms
AN	256K
BN	1060K
RN	2K
T	32.0 ms
I	102.3 mA

B. Single-Bank, CAS Latency 3, Burst Length 8, Organization x8

- tCK3 = 10 ns
- Constant access with 2K/32 ms Auto-Refresh
- CKE high; $\overline{CS}$ low

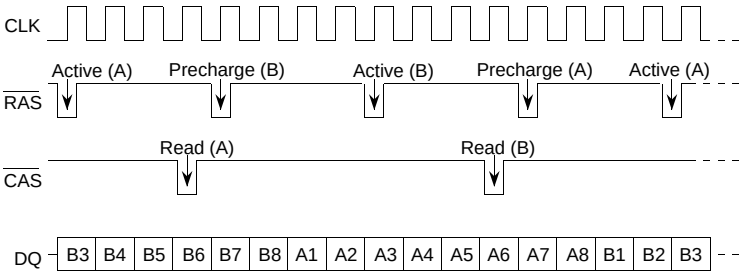


System Parameters

tCK	10 ns
tRAS	212K x 120 ns + 2K x 70 ns = 25.6 ms
tRP	32.0 ms – 25.6 ms = 6.4 ms
AN	212K
BN	1696K
RN	2K
T	32.0 ms
I	130.2 mA

C. Dual-Bank, CAS Latency 3, Burst Length 8, Organization x8, Ping Pong

- tCK3 = 10 ns
- Constant access with 2K/32 ms Auto-Refresh
- CKE high; CS low



System Parameters

tCK	10 ns
tRAS	32.0 ms – 2K x 50 ns = 31.9 ms
tRP	2K x 50 ns = 0.1 ms
CN	398K
DN	3180K
RN	2K
T	32.0 ms
I	218.5 mA

95YL-0594B (6/95)

Applications 9

The NEC synchronous DRAM is intended for designs that require bandwidths not easily achieved with asynchronous DRAMs. The threshold frequency at which synchronous designs have advantages over asynchronous designs depends on several factors.

(1) System Bus Width. Wider buses produce a higher bandwidth but add pins to the controller, complicate layout nets, and require additional real estate.

(2) Bus Bandwidth. A 64-bit-wide CPU fills the cache at a 66.7-MHz rate, requiring a transfer rate of 533.6 MB/s (or an 8-byte bus running synchronously at 66.7 MHz). The NEC synchronous DRAM covers both the interleave and linear burst sequences.

(3) Speed Upgrade. Planned future versions of the synchronous DRAM will extend the clock frequency well beyond 100 MHz, allowing improved performance over the product's life cycle.

(4) Simplification of the Memory Interface. The command structure of synchronous DRAMs simplifies the state machine design of the memory control interface. The dual-bank structure affords ready-made bank interleaving for gapless data I/O.

9.1 High-Performance Buffer Memory

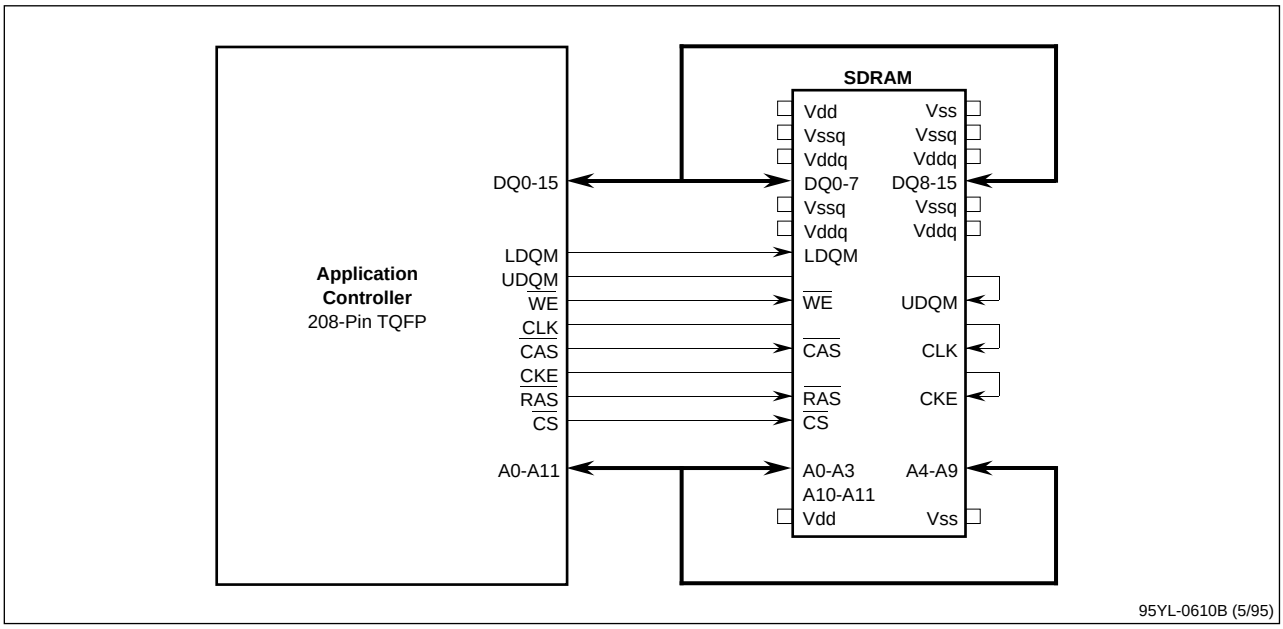
Lightly loaded systems (≤30 pF) can use simple, cost-effective source series terminations with short trace lengths to implement the system interface. Figure 9-1 is a typical block diagram of this application.

The 1M x16 SDRAM allows the option of creating a 200-MB/s peak transfer channel operating at 100 MHz. The 44-pin interface includes four pairs of power and ground pins. The memory can easily be expanded to 4 megabytes with the addition of another 1M x16 SDRAM and a $\overline{CS}$ output pin on the interface. If higher bandwidth is desired, the data bus can be widened by 16 bits for a 32-bit data I/O interface (adding 22 pins for a total of 66) and a peak bandwidth of 400 MB/s.

This application tightly couples the memory to the application and with proper design can utilize the dual banks to hide precharge, thus reaching the maximum usable bandwidth. The ideal applications include (1) Digital signal processors, (2) Local

memory for massively parallel processing, (3) ATM SARs, and (4) MPEG2 set-top decoders.

Figure 9-1. Single SDRAM Controller Application



9.2 Main Memory

9.2.1 Eight-Byte DIMM Presence Detect Pins

The application of synchronous DRAM to main memory requires the use of EIA/JEDEC standard 200-pin dual in-line memory modules (DIMM), buffered and non-buffered. Tables 9-1 through 9-2 tabulate the presence detect matrix PD1 through PD8 and hence the standard configurations possible.

Table 9-1. Presence Detect Pins PD8 - PD5

PD8	Byte Write	PD7	Buffered	PD6	PD5	Speed
1	Word	1	No	1	1	15 ns
0	Byte	0	Yes	1	0	12 ns
				0	1	10 ns
				0	0	8 ns

Table 9-2. Presence Detect Pins PD4 - PD1

PD4	PD3	PD2	PD1	DIMM Configuration	SDRAM	Rows	Columns
1	1	1	1	No Module			
1	0	0	0	1M x64/x72/x80	1M x16	12	8
0	0	0	0	2M x64/x72/x80	1M x16	12	8

Table 9-2. Presence Detect Pins PD4 - PD1 (cont)

PD4	PD3	PD2	PD1	DIMM Configuration	SDRAM	Rows	Columns
1	0	0	1	2M x64/x72/x80	2M x8	12	9
0	0	0	1	4M x64/x72/x80	2M x8	12	9
1	0	1	0	4M x64/x72/x80	4M x4/16	12	10
0	0	1	0	8M x64/x72/x80	4M x4/16	12	10
1	0	1	1	8M x64/x72/x80	8M x8	TBD	TBD
0	0	1	1	16M x64/x72/x80	8M x8	TBD	TBD
1	1	0	0	16M x64/x72/x80	16M x4	TBD	TBD
0	1	0	0	32M x64/x72/x80	16M x4	TBD	TBD
1	1	0	1	RFU	TBD	TBD	TBD
0	1	0	1	RFU	TBD	TBD	TBD
1	1	1	0	RFU	TBD	TBD	TBD
0	1	1	0	RFU	TBD	TBD	TBD
0	1	1	1	Expansion			

The buffered presence detect pins PD1 through PD8 are enabled by asserting the $\overline{\text{PDE}}$ pin to a logical low during the power-on reset sequence on a per- module basis. Note that a logical 1 on a presence detect pin is a no-connection, whereas a logical 0 is driven low when $\overline{\text{PDE}}$ is asserted low.

Buffered DIMMs (PD7 = 0) with byte-write (PD8 = 0) shall be capable of both word-write and byte-write operations; individual byte-mask (DQMBx) pins must also be buffered.

9.2.2 Identification Pins

Table 9-3 tabulates the Identification pin functions.

Table 9-3. Identification Pins ID2, ID1, ID0

ID2	Power	ID1	Precharge	ID0	Command Interval
1	Low-power (battery)	1	Early RAS	1	1 Clock
0	Normal	0	No early RAS	0	2 Clocks

The ID pins are left unbuffered so that the system will default to the module with the most constraining conditions (assuming that the ID bits of all modules are wired in series). As an example, the ID2 power pin would be worst case for normal refresh period SDRAMs, which do not have extended refresh as do low-power SDRAMs. In this case, the existence of a single “normal refresh module” requires the controller to ensure the shorter refresh period.

The read precharge ID1 bit involves the timing of a precharge at the end of a cycle. The JEDEC standard is no early-precharge, but some manufacturers have included it

in their SDRAM definitions. This is the number of clock cycles from the last burst-read data to the assertion of the precharge command.

The column-to-column interval ID0 bit is the number of cycles between random column read/write accesses. This can be done on every cycle (1 clock) in the NEC SDRAM definition.

9.2.3 Mechanical Keys

The module contains mechanical keys, which currently support only a 3.3-volt supply with LVTTL interfaces. Two supply voltages and two interface types are "Reserved for Future Use" (RFU).

9.2.4 Signal Pins

Table 9-4 defines pin functions on the 8-byte DIMM package.

Table 9-4. Eight-Byte DIMM Pin Functions

Pin Name	Number	Function
A0 ... A15*	16	Address Input (Multiplexed)
DQ0 ... DQ79	80	Data Input/Output (Common)
CLK0 ... CLK3*	4	Clock Input
CKE0 ...CKE3*	4	Clock Enable Input
$\overline{CS0}$ ...$\overline{CS3}$*	4	Chip Select Input
$\overline{RE}$*	1	Row Enable ($\overline{RAS}$)
$\overline{CE}$*	1	Column Enable ($\overline{CAS}$)
$\overline{WE}$*	1	Write Enable
DQM*	1	Data Mask (x64/x72/x80)
DQMB0 ...DQMB7*	8	Byte Data Mask
REGE	1	Buffer/Register Enable
$\overline{PDE}$	1	Presence Detect Buffer Enable
PD1 ...PD8*	8	Buffered Logical Presence Detect Output
ID0 ...ID2	3	ID Output
IN, OUT	2	Unbuffered Physical Detect Input/Output
Vdd	9	Power Supply
Vddq	20	Power Supply for Data Input/Output
Vref	2	Reference Power Supply
Vss	33	Ground
Vtt	11	Termination Power Supply
RFU	2	Reserved for Future Use

* Buffered

The number of pins listed in Table 9-4 totals 212. However, two pins are shared: A15 and A14 with $\overline{CS3}$ and $\overline{CS2}$. Also, the eight DQMB pins are alternatively used as DQ

pins; the DQMB function is not required on error detecting and correcting applications because the entire 80-bit data word is always read or written per access .

The IN and OUT pins are intended for use in a daisy chain interconnect to the controller and are shorted together on the module. In the system, the end of this trace is terminated at Vdd, indicating to the controller that a complete bank has been installed.

The number of power and ground pins is one-third of the pin count total. It is necessary to have a separate set of power and ground pins for the interface, which is satified by the 20 Vddq pins and 33 Vss pins. The nine Vdd pins supply the SDRAM memory arrays and are not subject to the current surges experienced on the high-speed output drivers.

Two Vref pins will supply the voltage reference level for input receiver comparators in future high-performance interfaces. Also, 11 Vtt pins are intended to supply the proper termination voltage for the transmission terminating resistors of this future interface.

9.2.5 Registered and Buffered DIMMs

The asterisks in Table 9-4 indicate on-module buffered signals. Clock CLK0 is buffered by a zero-delay, phase-locked loop that supplies multiple buffered in-phase clocks to the individual SDRAMs. See Figure 9-2. Note that each buffered clock drives only two loads. This ensures lightly loaded transmission lines to eliminate as much interdevice clock skew as possible, each line being the same net length.

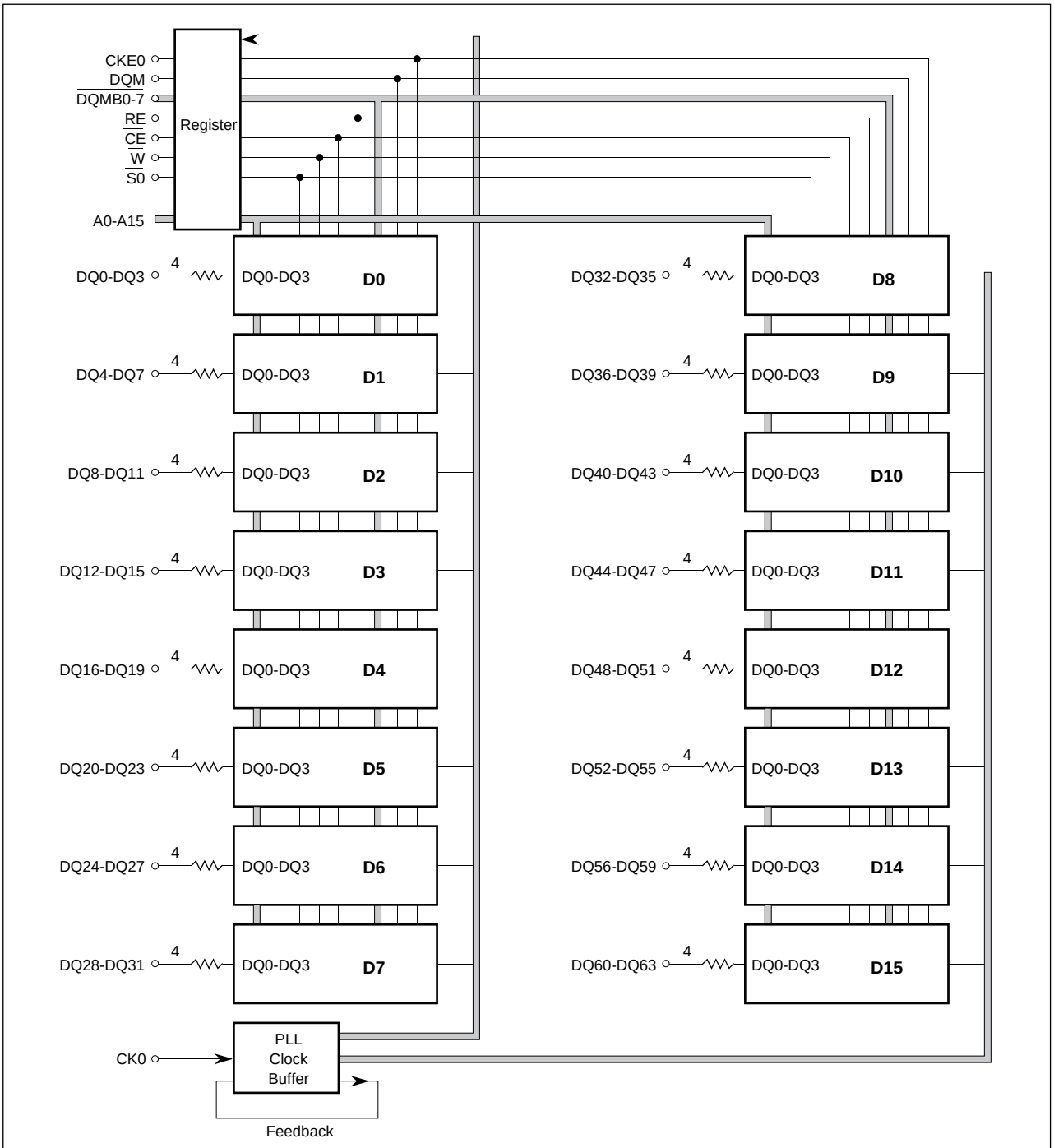
One buffered clock line drives the input signal registers/buffers. The device intended for the registers is 74AC11652 “Octal Bus Transceiver and Register with 3-State Outputs,” manufactured by Texas Instruments. The input pin REGE (Register Enable) is input to the SAB pin on the transceivers. The behavior of the transceiver is controlled by this input and acts either as a “real-time” data buffer (SAB asserted logical low) or as a register where the data is registered on the positive transition of the input clock (SAB asserted logical high).

The buffered DIMM stipulates a 10-ohm (±20%) series resistor for each DQ pin to control local stub reflections on the transmission line.

At the 16-megabit density, only addresses A0 through A11 need to be buffered, allowing room for other input signals. (Note that CLK0 is separately buffered by the PLL zero-delay buffer.) If the application does not require byte read or write, then the buffering of the eight DQMB pins can be eliminated. Texas Instruments manufactures a x18 Register, part number 74ALVC16835, that can buffer all required inputs. Most

modern workstation-level RISC CPUs do not utilize byte reads or writes and thus can capitalize on this cost reduction.

Figure 9-2. Buffered x64 DIMM; One Bank with x4 SDRAMs



Notes:
1. This configuration incorporates Word and Byte Write
2. A 10-ohm ± 20% resistor shall be wired in series with all DQn lines near the card edge connector.
3. All clock lines from the PLL Clock Buffer shall be of equal length.

95YL-0589B (6/95)

9.2.6 Unbuffered Eight-Byte DIMMs

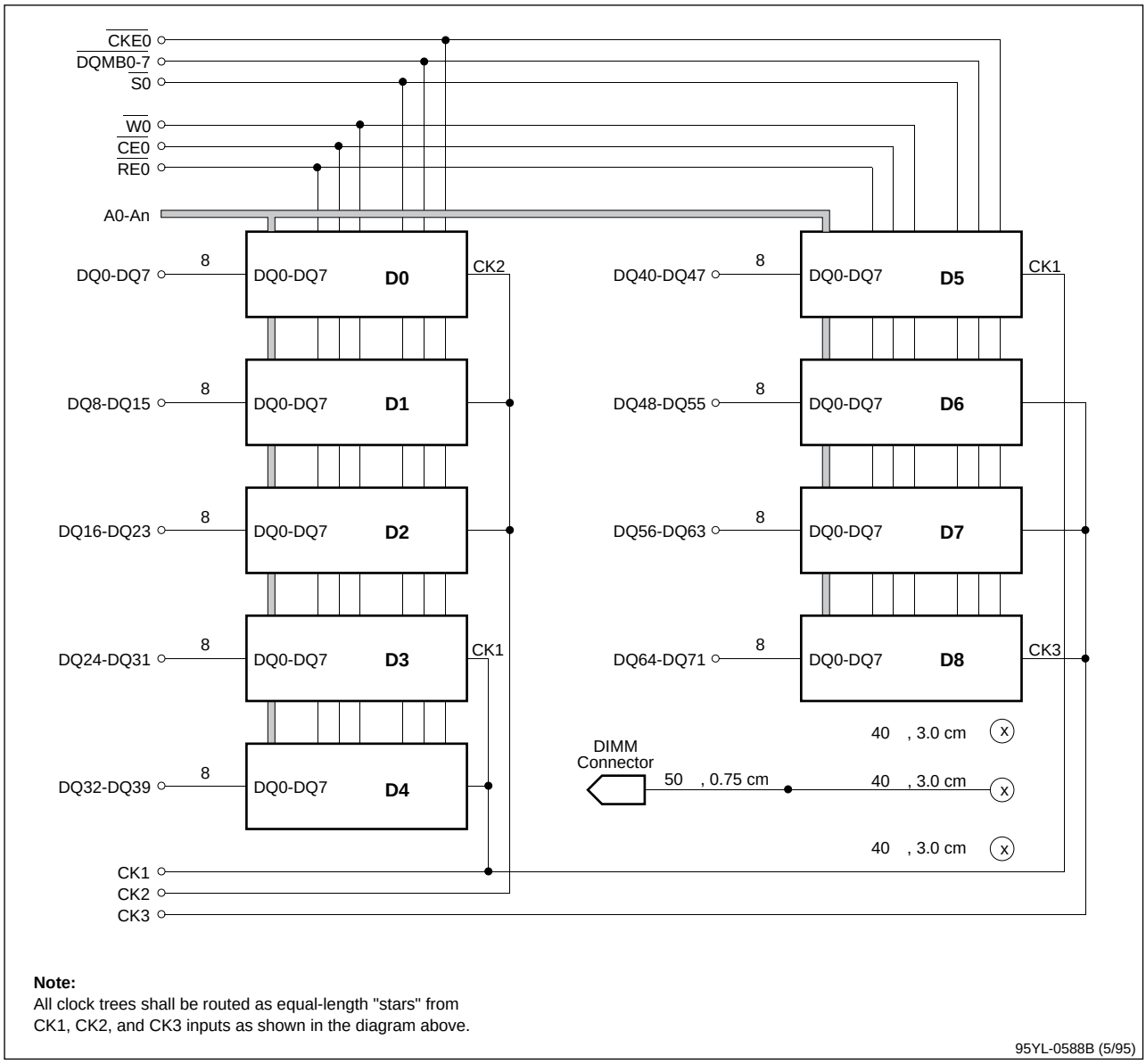
Unbuffered SDRAM DIMMs offer the simplest solution for an actual memory module but add further complexity at the motherboard and controller level. Therein lies the tradeoff that must be made. The module does not include any buffering of input signals nor any clock regeneration, thus saving cost. The alternative is that the maximum number of loads is multiplied by each additional module loaded into the system.

The unbuffered SDRAM DIMM is limited to systems where the total number of modules does not exceed four. Buffering the major input signal groups must be accomplished by the memory controller or by discrete buffers on the motherboard. The issue at this point is one of cost from the “As Shipped Memory Load” versus granularity and the cost of upgrading the system memory. The optimum solutions use the 1M x16 and the 2M x8. The 4M x4 requires a minimum of 16 devices per module for a x64 configuration. A four-module system configuration would require a driver capable of driving a 300-pF load on the address and control signal buses. It is possible according to the JEDEC standard but does not seem very practical.

Clock distribution (Figure 9-3) to the unbuffered DIMM becomes extremely important because each clock has to support a minimum of three loads (single bank) per module versus a single load in the buffered DIMM. Routing is specified in the standard to control the net length and ohmic value of the transmission line. The worst case dual-bank module requires each clock to support a minimum of six loads per module, severely limiting the maximum number of modules.

Another question is whether future system upgrades are to be offered. The unbuffered DIMM limits performance to a maximum of 66.7 MHz, with higher frequency upgrades being difficult or impossible to design without major system changes.

Figure 9-3. Unbuffered x72 DIMM; One Bank With x8 SDRAMs



Note:
All clock trees shall be routed as equal-length "stars" from CK1, CK2, and CK3 inputs as shown in the diagram above.

95YL-0588B (5/95)

9.2.7 Unbuffered vs Buffered DIMMs

The decision to use unbuffered over buffered DIMMS is derived from the present and future system requirements and the considerations in Table 9-5.

Table 9-5. Comparison of Unbuffered and Buffered DIMMs in System Design

	Clock Lines	External Drivers	Max Freq	Module Cost	Max Modules	Memory Load, MB	System Cost	SDRAM Config
Buffered	Single	Not required	83 MHz	Moderate	8	8 to 264	Moderate	4M x 4 2M x 8 1M x 16
Un-buffered	Multiple	Required	66.7 MHz	Lower	4	8 to 64	Lower	2M x 8 1M x 16

9.2.8 Eight-Byte DIMM Motherboard Layout

General guidelines in Chapter 3 apply to both the buffered and unbuffered DIMMs Only the buffered DIMM is discussed here.

Modeling of the data bus has to include the following real system path impedances:

- Driver IC pin inductance
- Driver board microstrip stub-to-edge connector
- Edge connector impedance
- Backplane microstrip or stripline impedance
- Edge connectors and stub discontinuities (i.e. throughholes)
- Receiver edge-connector/board-stub/IC-input pin

The use of microstrip is recommended for the motherboard interconnect because of its better propagation characteristics. Termination of the motherboard transmission lines to cancel reflections can be accomplished by one of the methods described below and shown in Figure 9-4.

(1) Source Series Termination

Source series termination (Figure 9-4A) can be used only in lightly-loaded systems (four loads maximum). The value is selected so that the internal source impedance added to the series resistance value equals the line characteristic impedance (Rsource + Rseries = Zo). The traces to the loads should run in parallel. In the case of four parallel transmission lines, the series value is selected so that the internal source impedance added to the series resistance value equals one-fourth of the characteristic impedance (Rsource + Rseries = Zo/4).

(2) Parallel Termination

Parallel termination can be used in systems with moderate to heavy loads; it depends mainly on the output drive available to drive the transmission line. Parallel termination can be accomplished through several different methods.

(3) Symmetrical Parallel Temination

Figure 9-4B requires the generation of a termination voltage that is one-half of Vdd. The terminating parallel equivalent resistance value must equal the transmission line characteristic impedance (Rt = Zo). Note that this can also be accomplished by using two resistors in a divider network between Vdd and ground. The values chosen for the terminating pair must in their parallel equivalent value equal the transmission line characteristic impedance.

(4) Symmetrical Double-Parallel Termination

Figure 9-4C terminates both the near and far ends of the transmission line. The parallel terminating resistor values must equal the transmission line characteristic impedance (R1:R2 = Zo). Again, this technique requires the generation of a terminating voltage, Vtt.

(5) Asymmetrical Parallel Termination

Figure 9-4D terminates the far end of the transmission line through a single resistor pulled up to Vdd. The resistor value must equal the transmission line characteristic impedance (Rt = Zo).

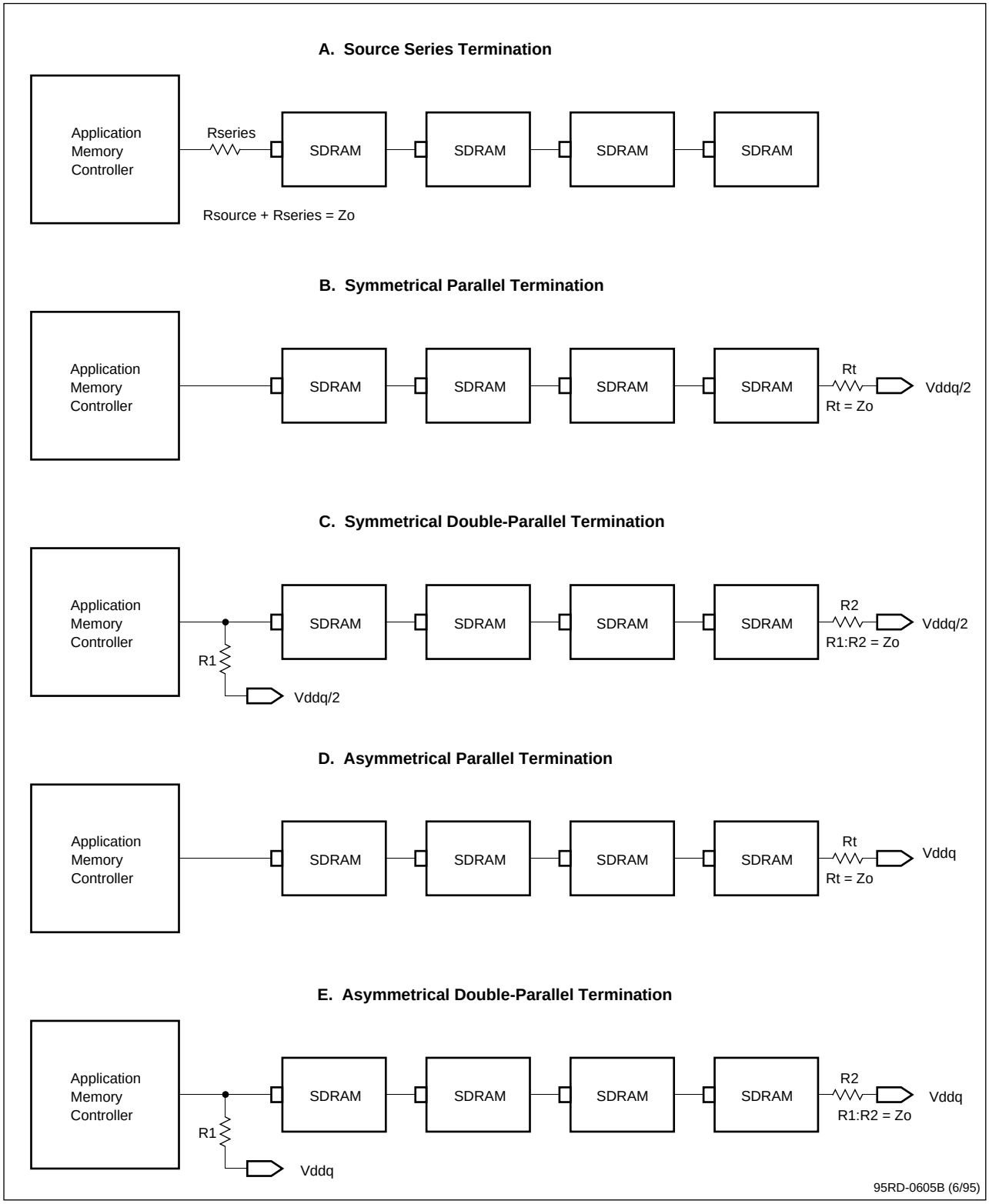
(6) Asymmetrical Double-Parallel Termination

Figure 9-4E terminates both the near and far ends of the transmission line through resistors pulled up to Vdd. The parallel terminating resistor values must equal the transmission line characteristic impedance (R1:R2 = Zo).

(7) Power Considerations

The terminating technique selected must take certain other factors into account. Power dissipation, for instance, is lowest in the source series termination because power is expended only during switching transients and very little current is drawn in the quiescent state. Generation of Vtt requires voltage regulation, but power requirement is low.

Figure 9-4. Transmission Line Termination



NEC

VHDL/Verilog Model from RAVIcad A

A.1 Overview

The fully developed SDRAM model emulates both the functionality and timing of the actual device with all input signals synchronized to an external clock. Memory density of the device is 16M bits, which is available in three organizations: 4M x4, 2M x8, and 1M x16. The memory itself is divided into two banks. There are 4096 memory pages with each bank having 2048 pages.

Commands are given to the SDRAM by a combination of input signals RAS, CAS, WE, CS, DQM (all active-low), and CKE. The state of these signals is read on the rising edge of the clock. Typical commands are activate, read, write, precharge, and refresh. Programmability is provided to set the $\overline{\text{CAS}}$ latency, burst length, and wrap sequence (sequential/interleave). A mechanism for byte control also is available. Refreshing may be accomplished by either CBR command that internally generates the refresh address or a self-refresh command that internally generates the refresh address and the timing to automatically execute the cycle.

A.2 Features

- Functional checking for illegal states as defined in the NEC data sheet
- Timing checking for setup, hold, pulse width, and command period violations
- User-selectable access times for 10, 11, 12, and 13 ns
- User-selectable organizations (x4, x8, x16) with byte control
- Multiple instances of model
- Built-in system debugging features
- Dynamic memory allocation in VHDL
- Static or hash table implementation in Verilog
- Memory dump sheme

A.3 Special Features

There is an option to load data into the memory from disk space for read/write operations whenever it is required. Before accessing a new page from the disk, the current page gets saved. The information regarding the saved pages is stored in a file. This saving of data is also available during a “dump” operation. The user has a provision to preload the memory with a set of data values.

A dynamic memory allocation scheme is implemented in the VHDL model in which memory pages are loaded at the start of simulation. The memory is treated as a component that is instantiated in the main model.

The Verilog model can use either a static memory or hash table as the memory module. It takes care of all memory-related operations. The memory component is declared as a module in the main model. The hash table scheme is implemented so that the user can initialize a small section of memory while maintaining efficient memory utilization.

A.4 Usage of Model in the User’s Test Bench

```
entity user_test_bench is
end;
architecture behavior of  user_test_bench is
-- Instantiate user’s component
component user_component
        generic (
                    . . .
                  );
        port  (
                  . . .
                );
end component;
-- Behavior of the SDRAM conforming to NEC Data Sheet, Ver. 4.0, March 31, 1994
component necsdram
              port (
                . . .
               );
end component;
signal  . . . ;
. . .
begin
U1 : user_component
```

```
        generic map (
                        . . .
                        )
port map (
                    . . .
                   );
U2 : necsdram
       port map (
                   . . .
                  );
end behavior;
configuration user_config of user_test_bench is
       for behavior
           for U1 : user_component
               use  configuration work. . . . .;
            end for;
           for U2 : necsdram
               use  configuration work.necsdram;
            end for;
       end behavior;
end user_config;
```